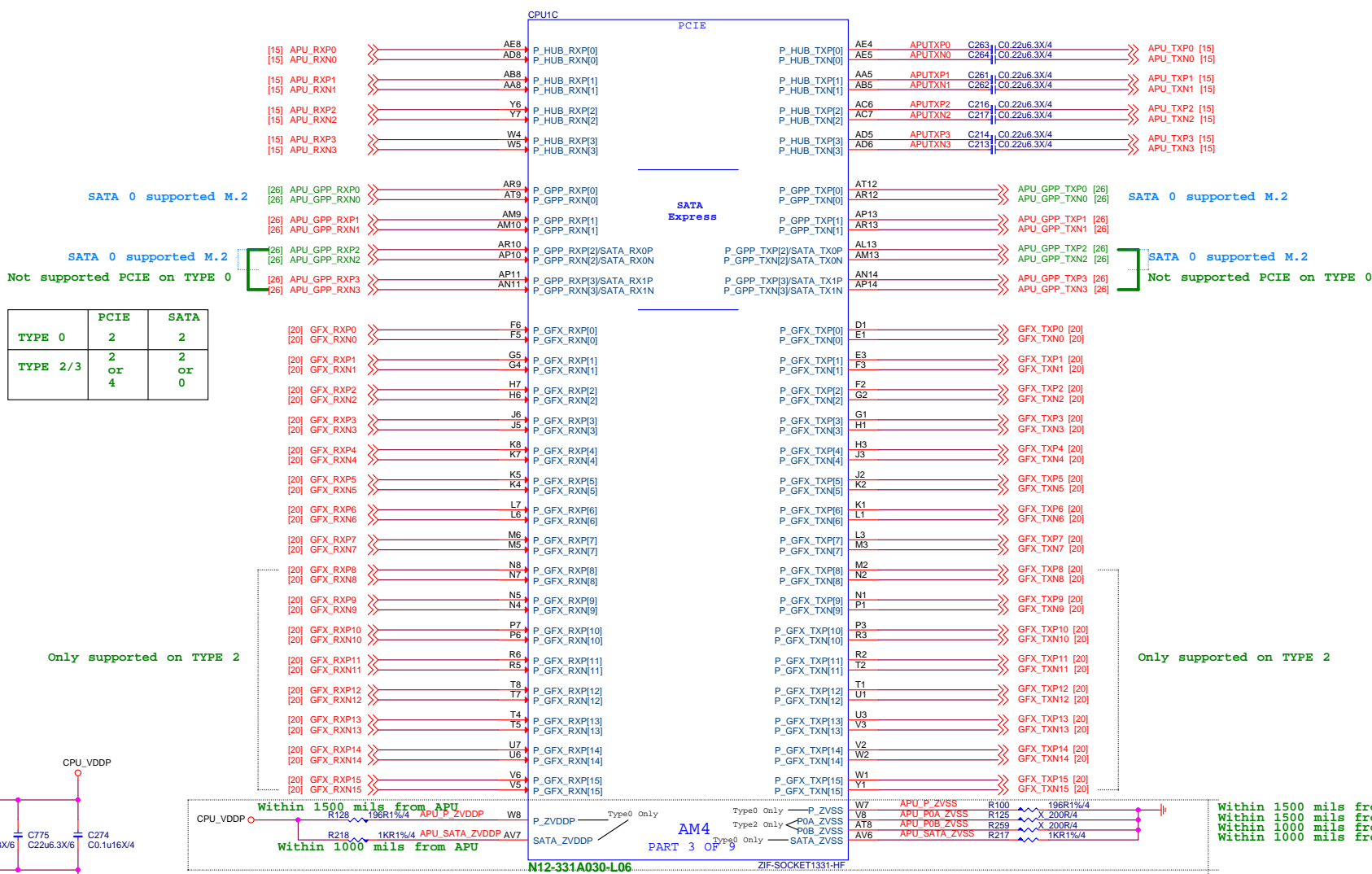
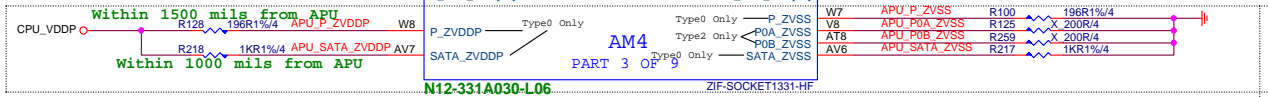
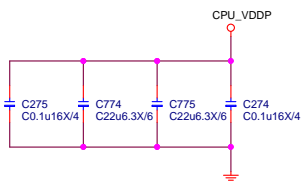



01 Cover Sheet	37 Front USB3.0 90° Header
02 Block Diagram	38 Front USB3.0 180° Header
03 FM4 DDR4 I/F	39 DVI
04 AM4 PCIE/SATAE	40 VGA
05 AM4 Display/Audio	41 HDMI
06 AM4 SVI/ACPI/GPIO	42 5VDIMM/3VSB
07 AM4 LPC/SPI/USB/CLK/STRAP	43 DDR VPP25/VTT
08 AM4 Power/VDDIO_AUDIO Power	44 DDR Power-RT8125E
09,10 RTC/Clear CMOS/RTC Power/GND	45 CPU 1.8_S0/S5
11,12,13,14 DDR4-POWER/GND	46 CPU VDDP-RT8125E
15 Promontory-PCIE/SATA/SATAE	47 CPU RT8894 4+2
16 Promontory-USB/OC	48 CPU Phase1-3
17 Promontory-CLK/ACPI/GPIO	49 CPU Phase4
18 Promontory-Power / 19 Promontory-GND	50 CPU NB
20 PCIE X16	51 CPU NB_S5
21 PCIE X1/PCIE X4	52 Prom-GS7133/2.5V
22 ASM1083 PCI Bri.	53 Prom-NB681/1.05V
23 PCI Slot	54 CPU Connector/PWRGD
24 SIO NCT6795D	55 ATX/Front Panel
25 HWM/COM/Debug LED	56 ALL LED Control
26 M.2	57 LED/OV Control
27,28 FAN 1/FAN 2	58 EMI CAP
29 LAN 8111H	59 BOM Option
30 Audio ALC892	60 Manual Parts
31 Audio De-POP	
32 USB Power	
33 Rear USB	
34 TYPE-A (USB3.1)	
35 Rear USB3.1 TYPE C	
36 Front USB2.0	



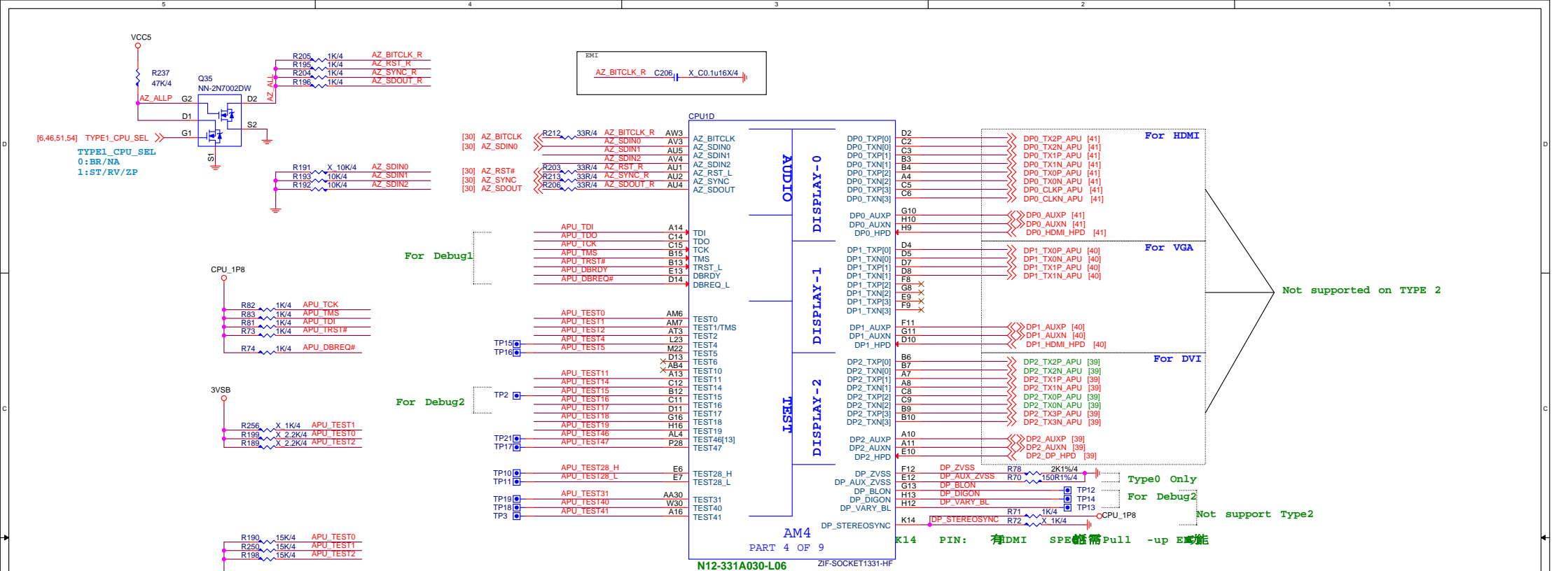
	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

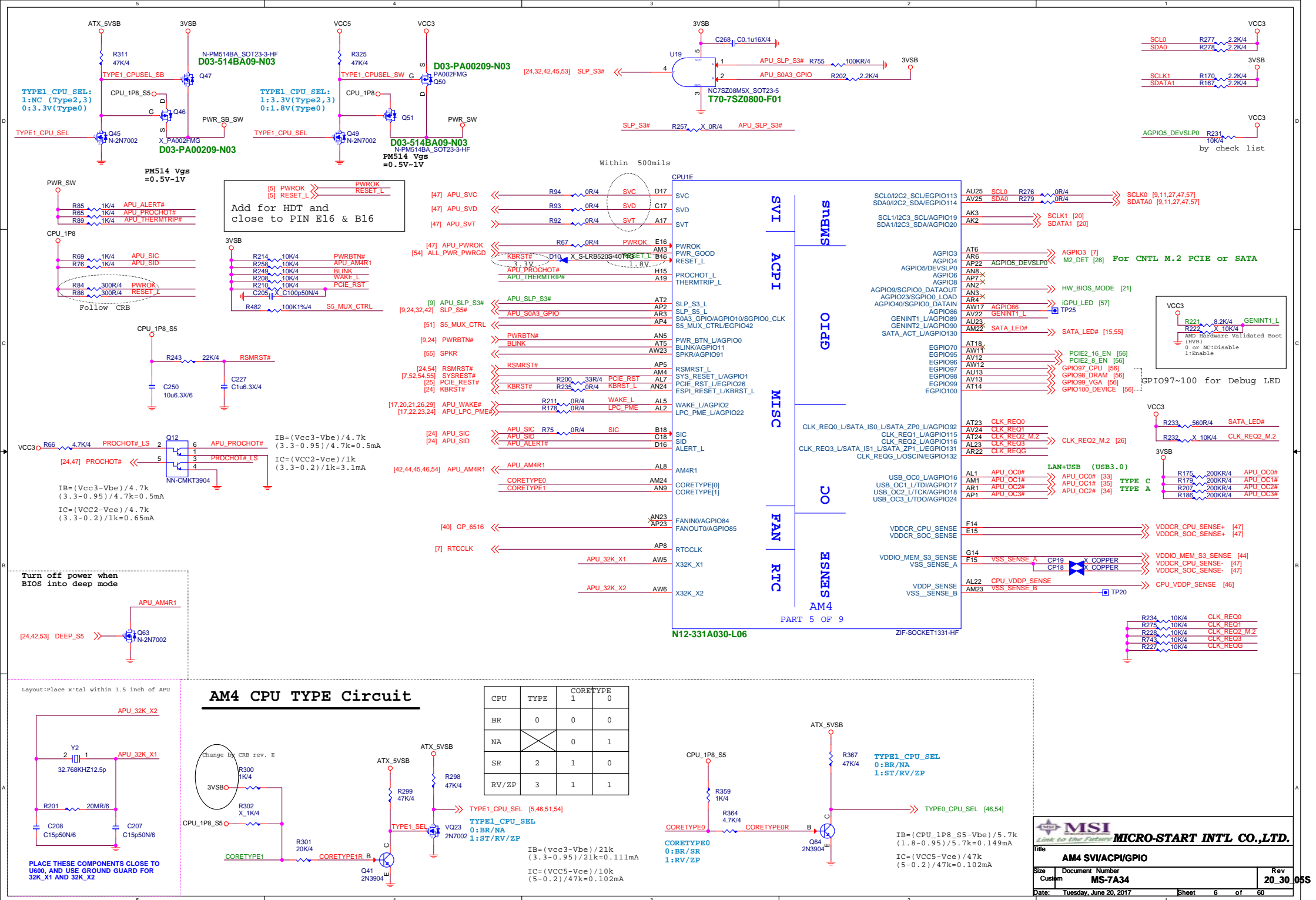


Vinafix.com

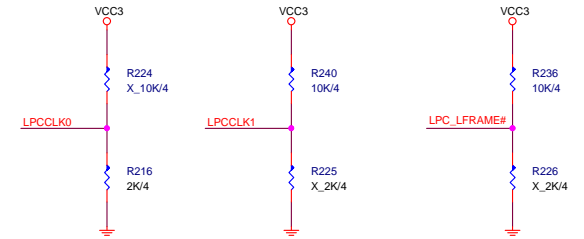
**MICRO-START INTL CO.,LTD.**

Title AM4 PCIE/SATAE		
Size Custom	Document Number MS-7A34	Rev 20_30_05S
Date: Tuesday, June 20, 2017		Sheet 4 of 60

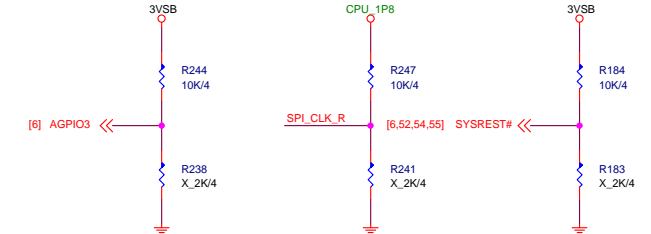




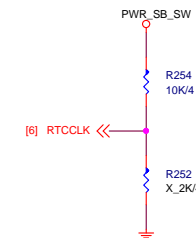
Strapping Options



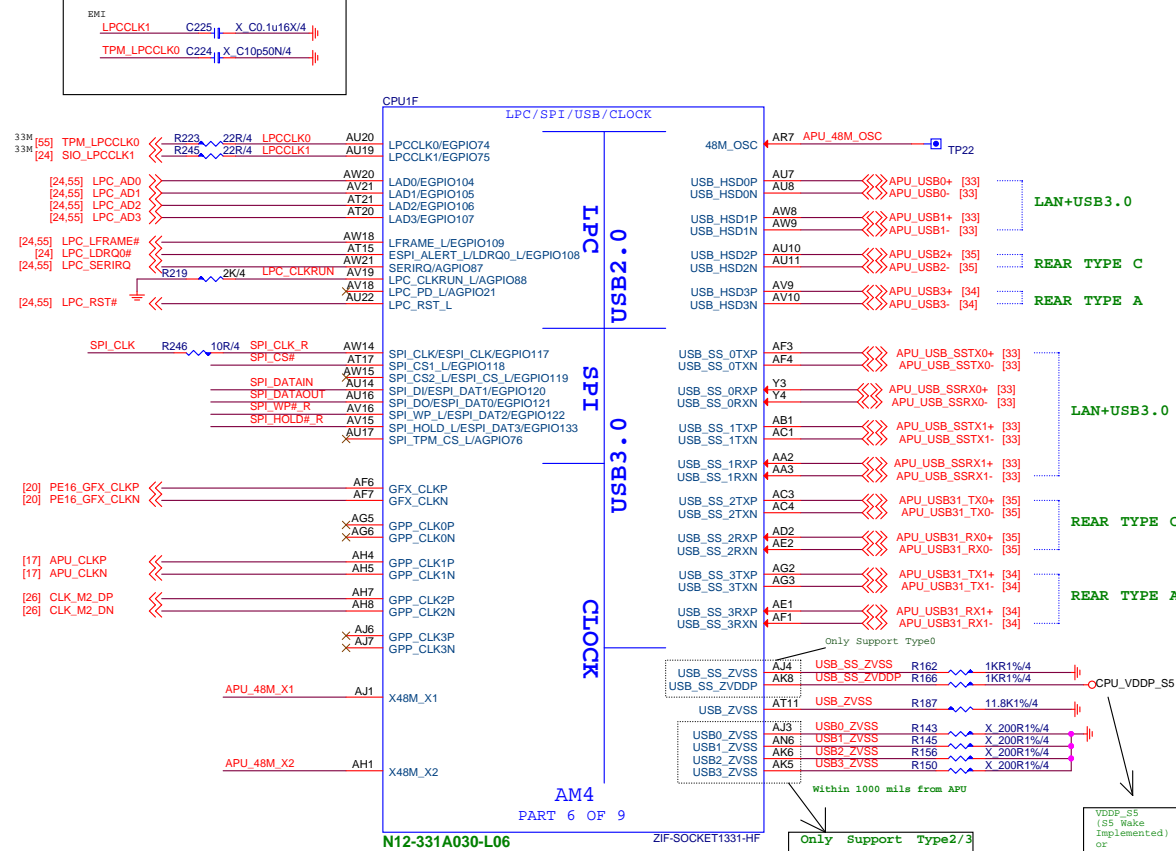
	LPCCLK0	LPCCLK1	SIO_LFRAME
PULL HIGH	LPC device Boot Fail Timer Enabled	Configured for Internal clock generator (Default)	SPI ROM (Default)
PULL LOW	LPC device Boot Fail Timer Disabled (Default)	Configured for External clock generator ?????	LPC ROM



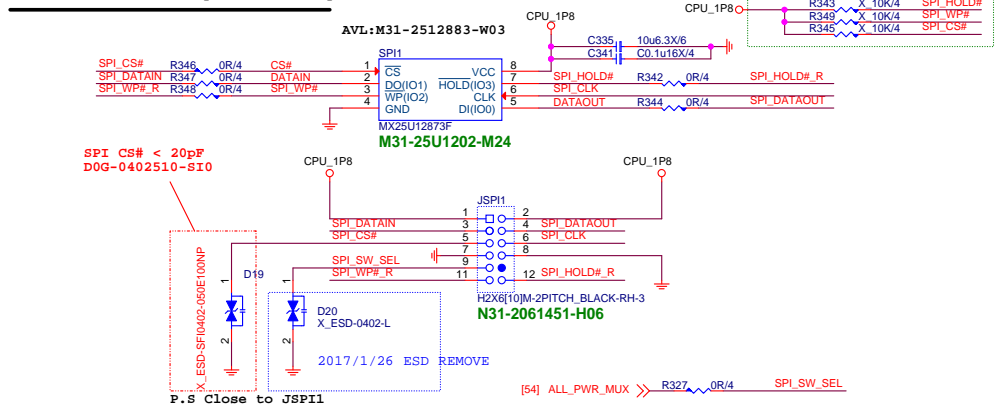
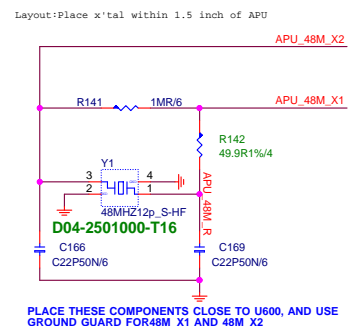
	AGPIO3	SPI_CLK	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	short reset mode



	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board



SPI ROM(1.8V)



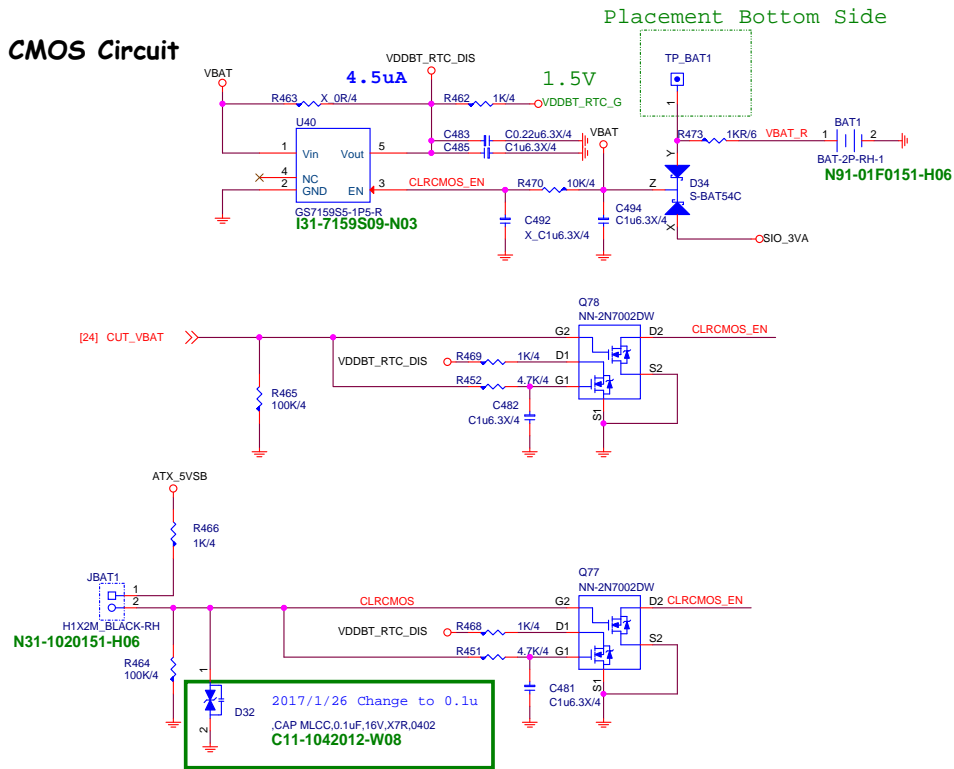
1.5V@0.25A



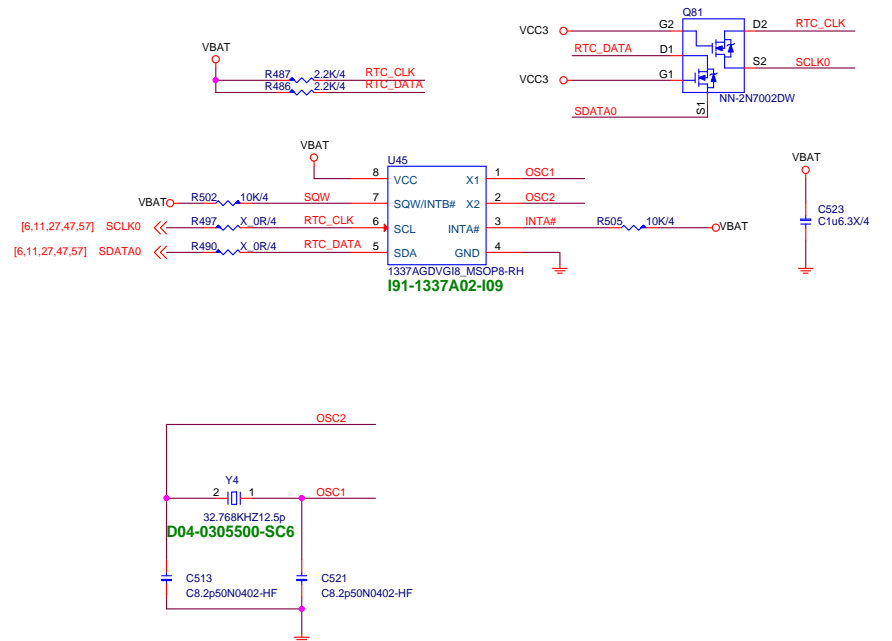
VCORE



RTC & Clear CMOS Circuit



For RTC

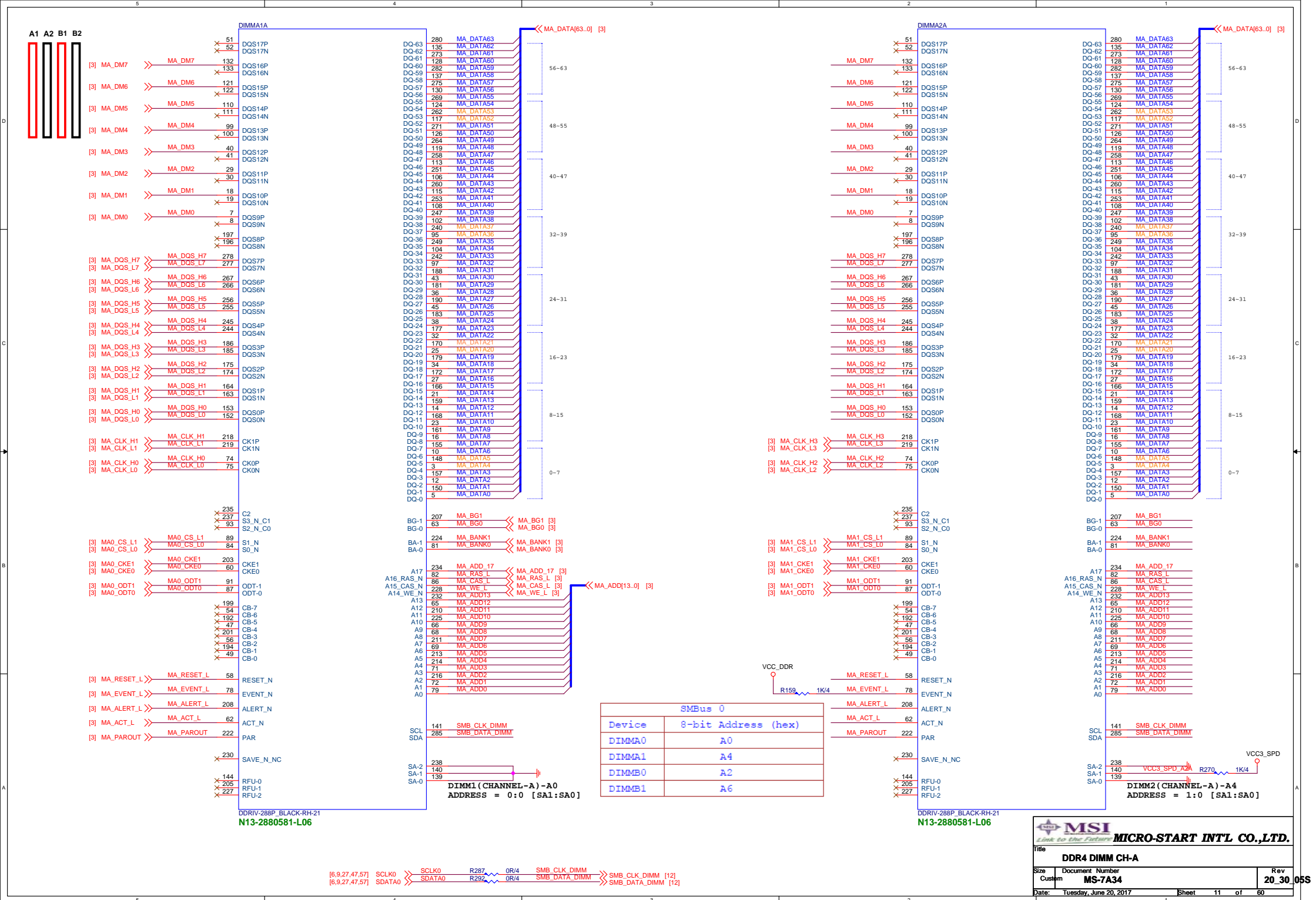


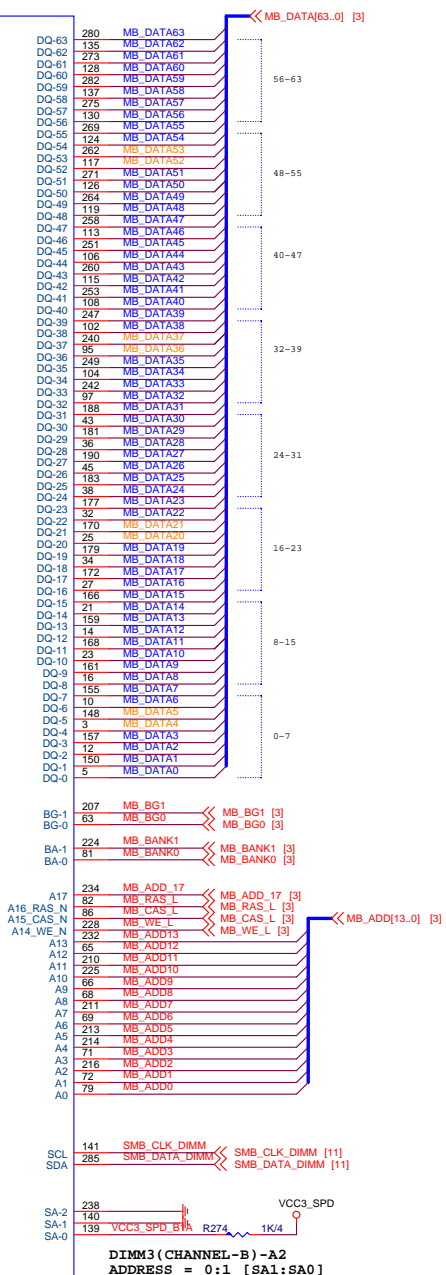
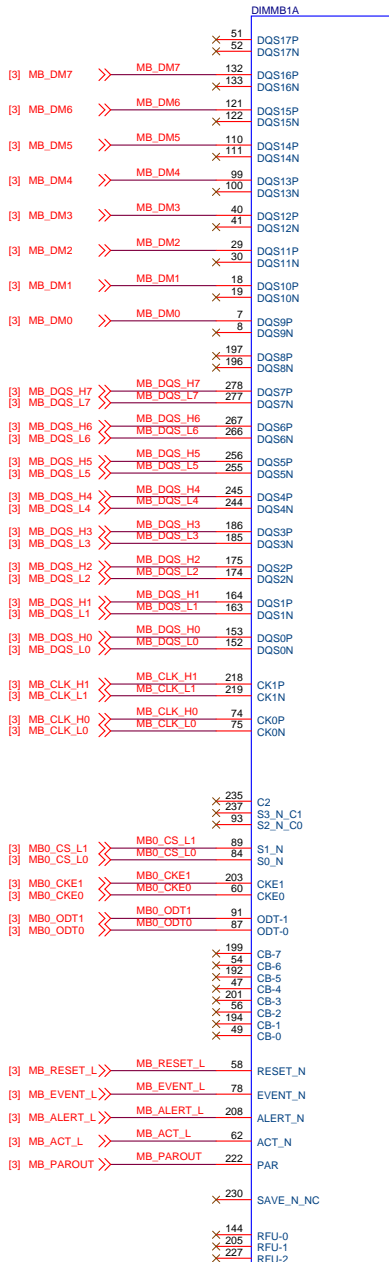
Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

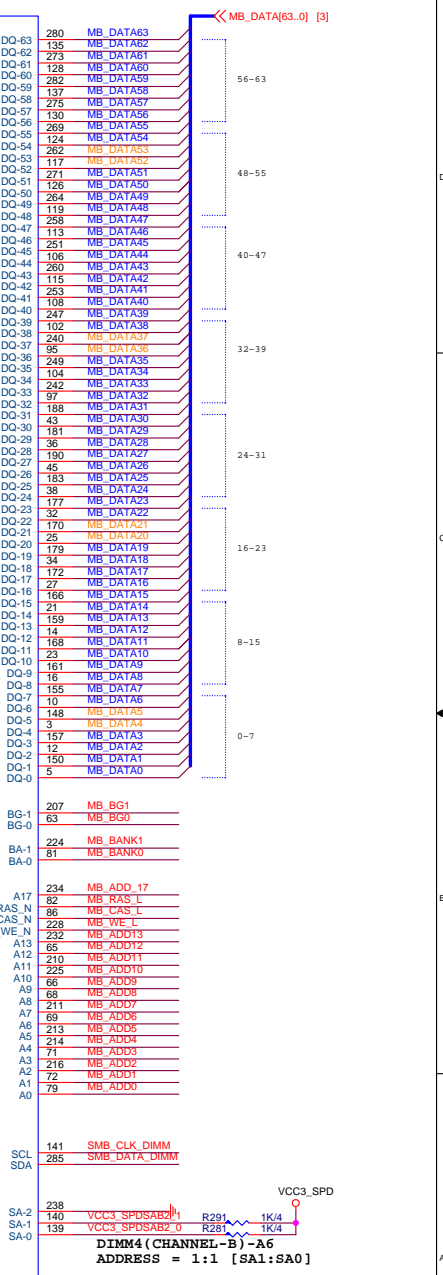
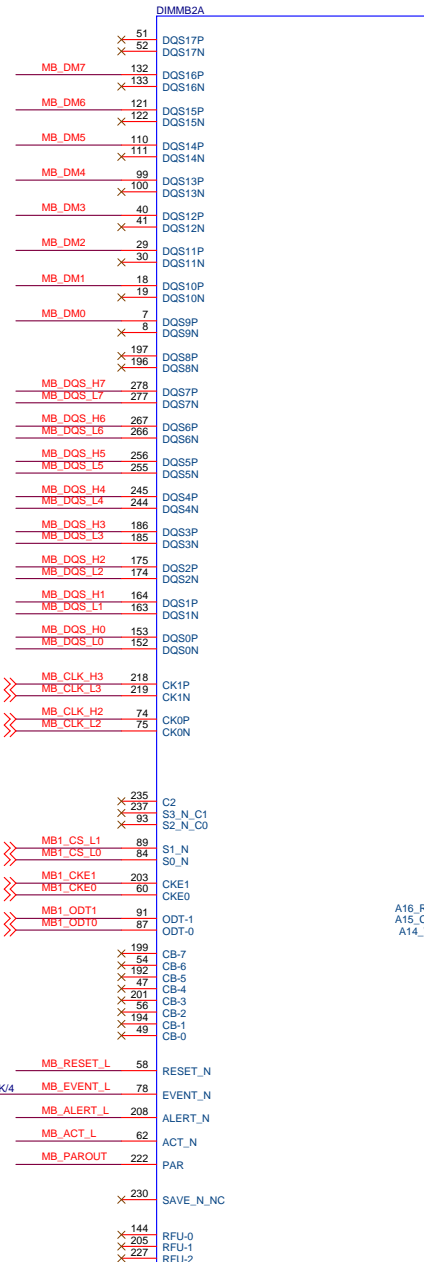
GND

AM4
PART 9 OF 9






DDRIV-288P_BLACK-RH-21
N13-2880581-L06



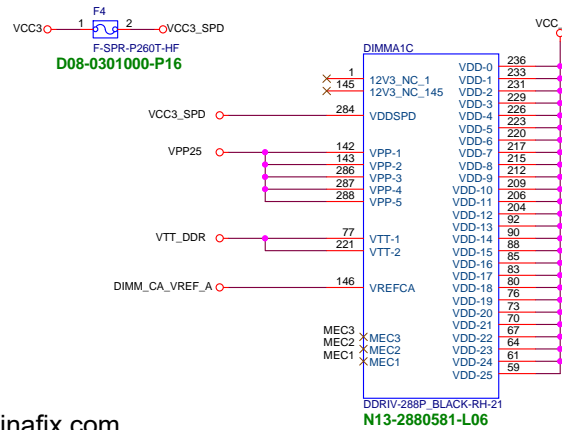
DDRIV-288P_BLACK-RH-21
N13-2880581-L06

MSI
Link to the Future
MICRO-START INTL CO.,LTD.

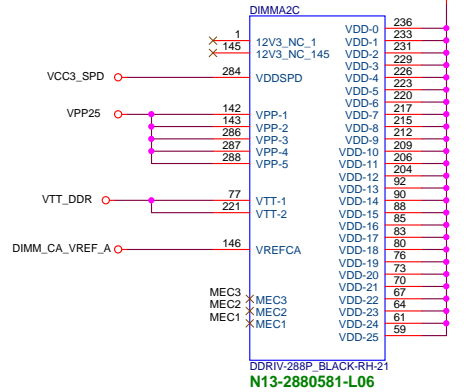
Title DDR4 DIMM CH-B		
Size Custom	Document Number MS-7A34	Rev 20_30_05S
Date Tuesday, June 20, 2017	Sheet 12	of 60

VCC3 — 1 —  — 2 — VCC3_SPD

F4
F-SPR-P260T-HF
D08-0301000-P16

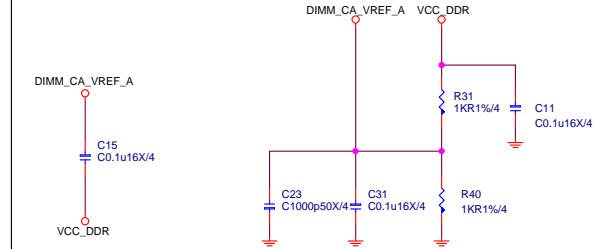


DIMM SLOT PN BY SPEC

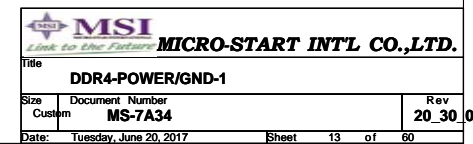
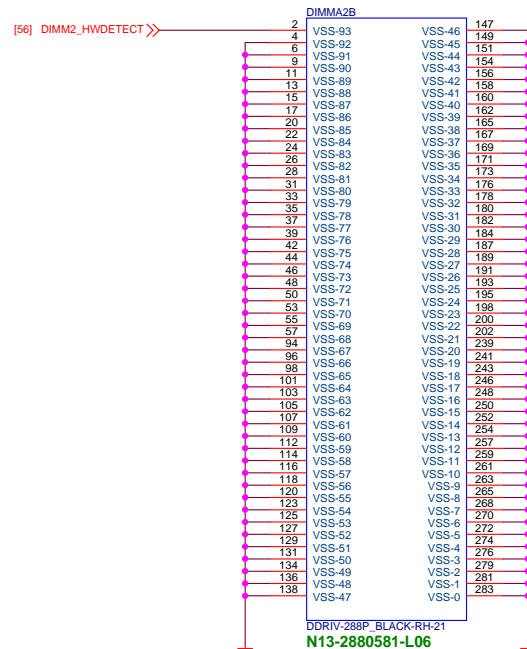
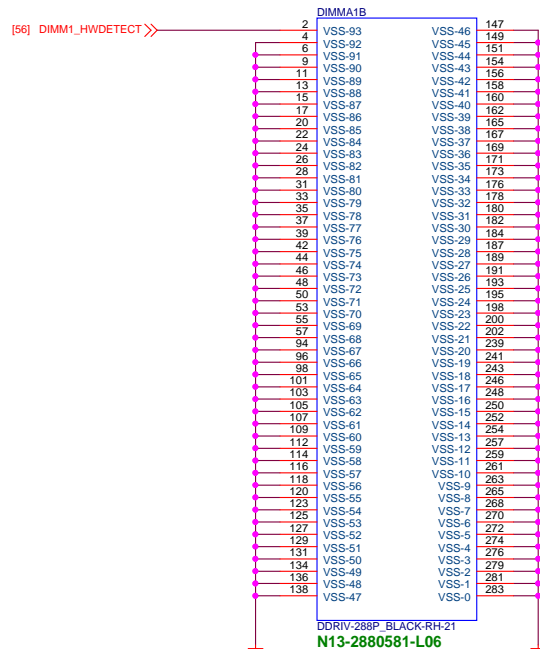
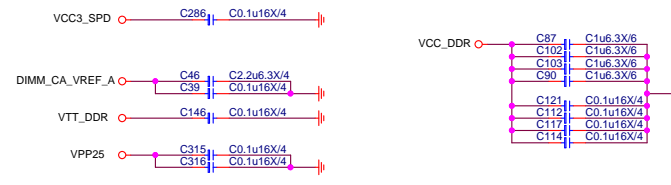
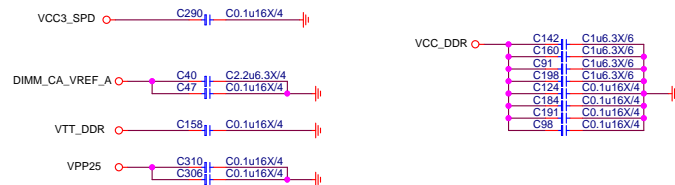


DDR VREF

(place resistors close to DIMMs)

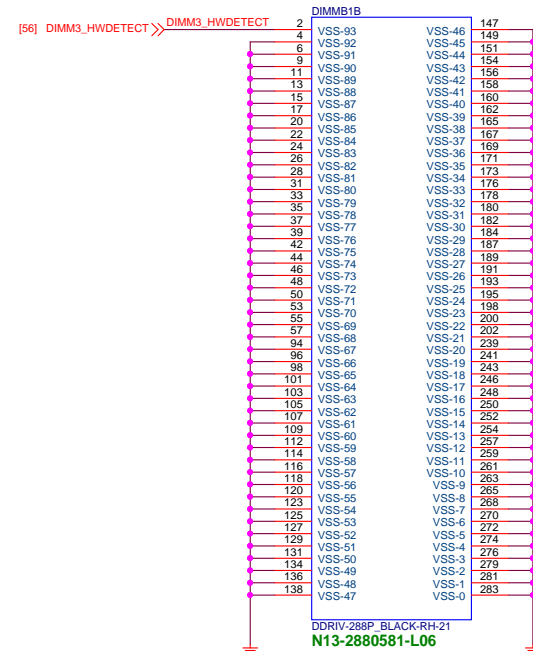
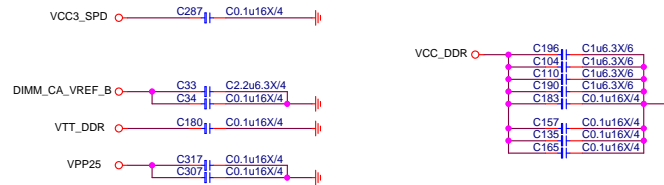
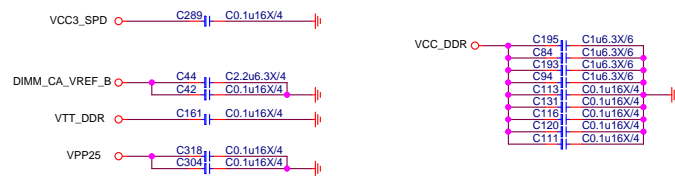
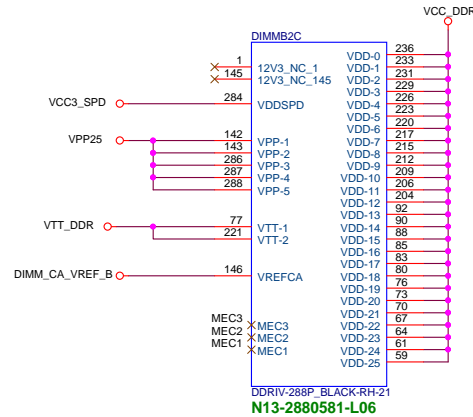
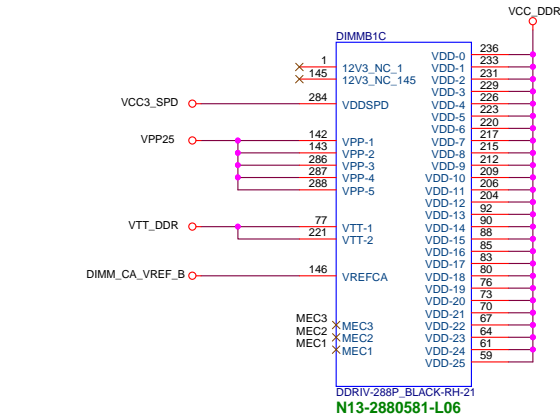
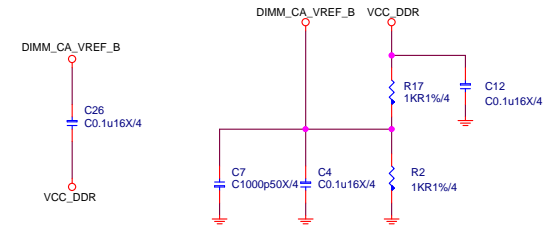


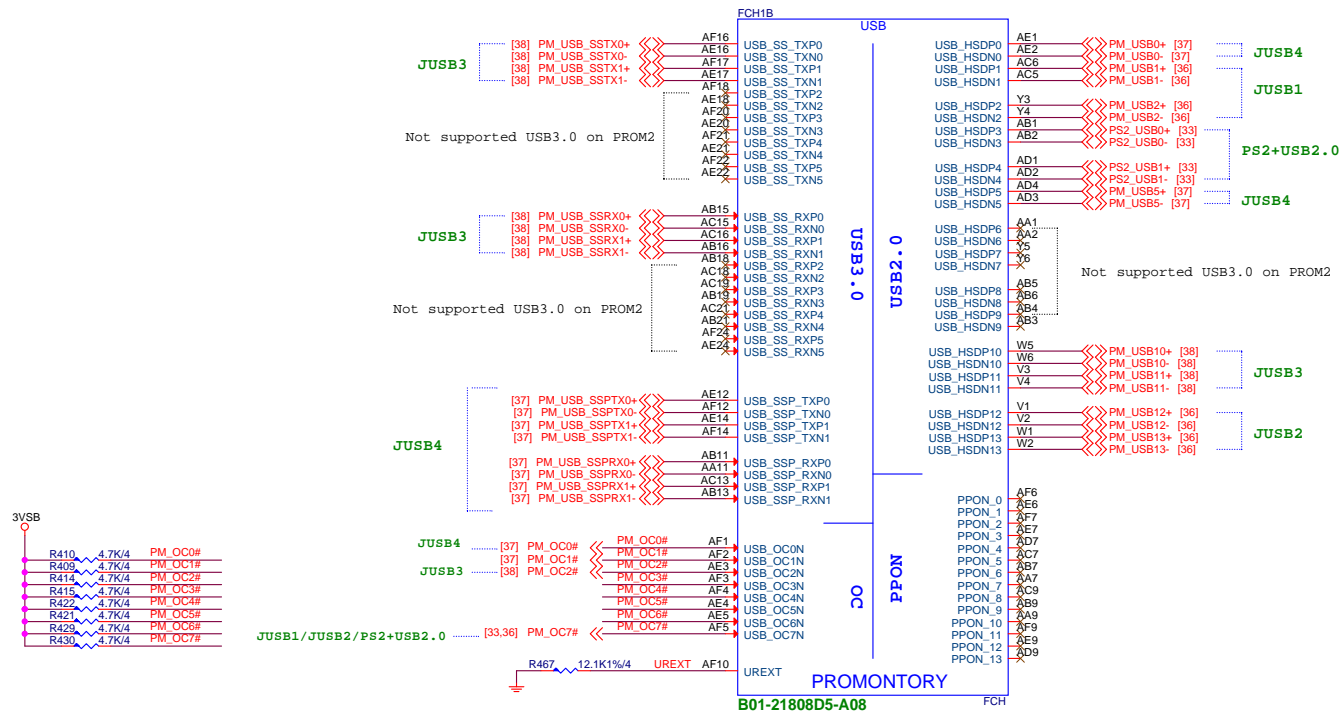
Vinafix.com



DDR VREF

(place resistors close to DIMMs)





Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

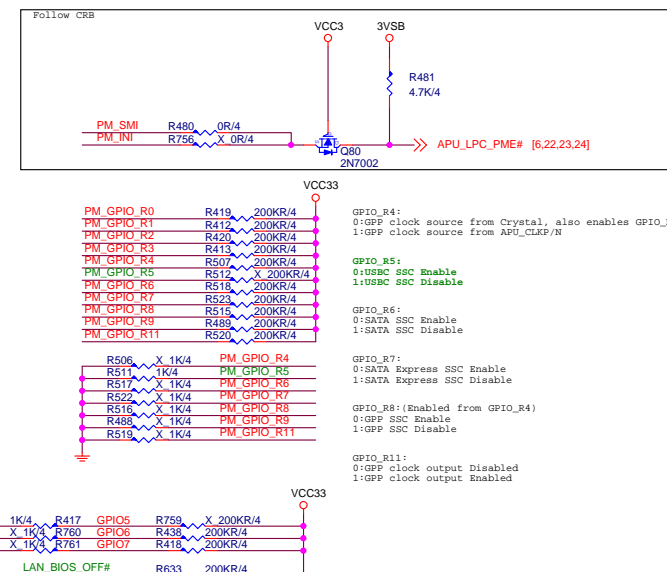
CLK2.3不能用
CLK1-3不能用

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0	USB_HSD Port0~5	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen1 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1	CLK0~1
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7


CLK2.3不能用
CLK1.3不能用

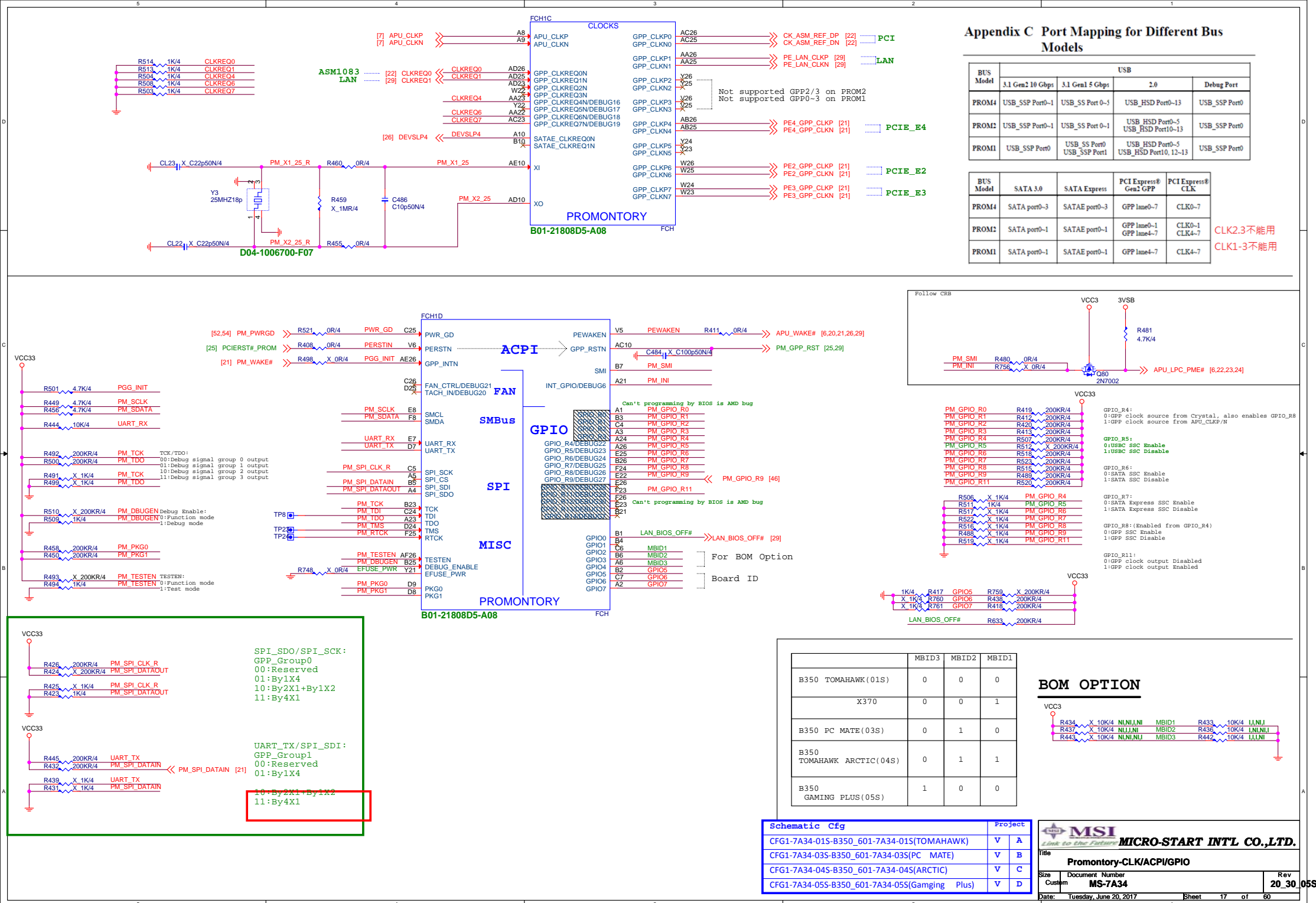


BOM OPTION

	MBID3	MBID2	MBID1
B350 TOMAHAWK (01S)	0	0	0
X370	0	0	1
B350 PC MATE (03S)	0	1	0
B350 TOMAHAWK ARCTIC (04S)	0	1	1
B350 GAMING PLUS (05S)	1	0	0

Schematic Cfg	Project
CFG1-7A34-01S-B350_601-7A34-01S(TOMAHAWK)	V A
CFG1-7A34-03S-B350_601-7A34-03S(PC MATE)	V B
CFG1-7A34-04S-B350_601-7A34-04S(ARCTIC)	V C
CFG1-7A34-05S-B350_601-7A34-05S(Gaming Plus)	V D

 MSI <i>Link to the Future</i>			MICRO-START INTL CO.,LTD
Title			
Promontory-CLK/ACPI/GPIO			
Size	Document Number	Rev	
Custom	MS-7A34	20_3	

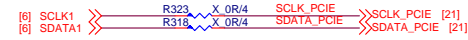
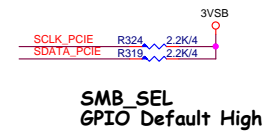
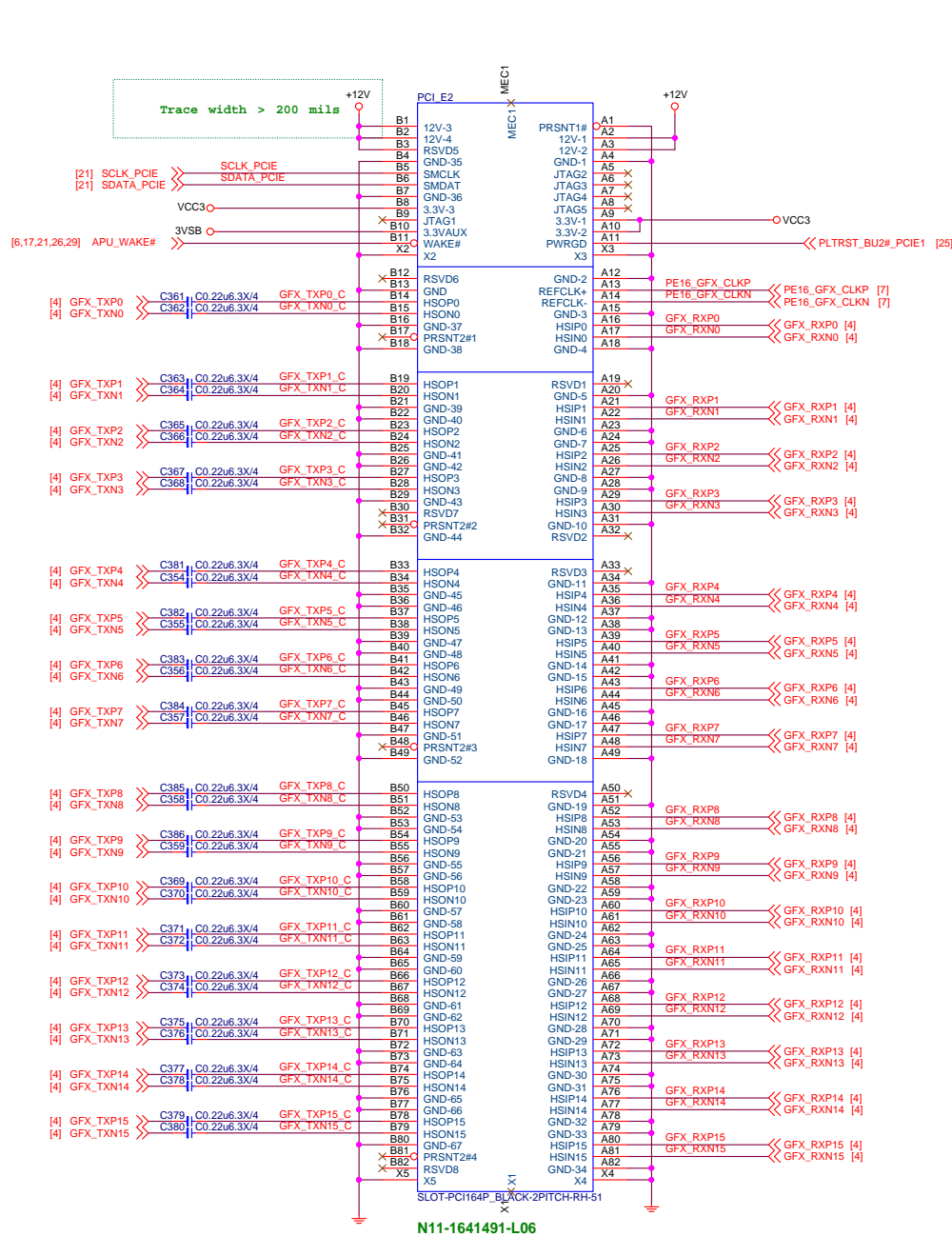


GND

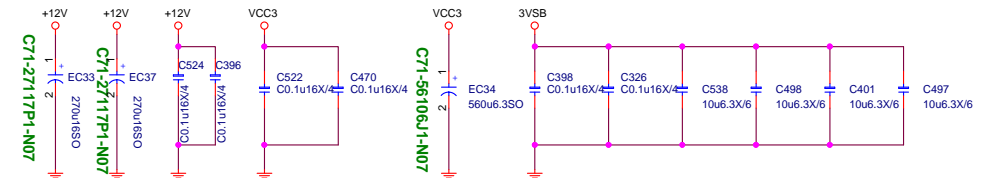
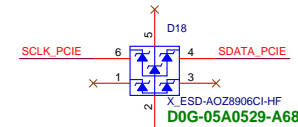
PROMONTORY

B01-21808D5-A08

PCI EXPRESS x16 Slot



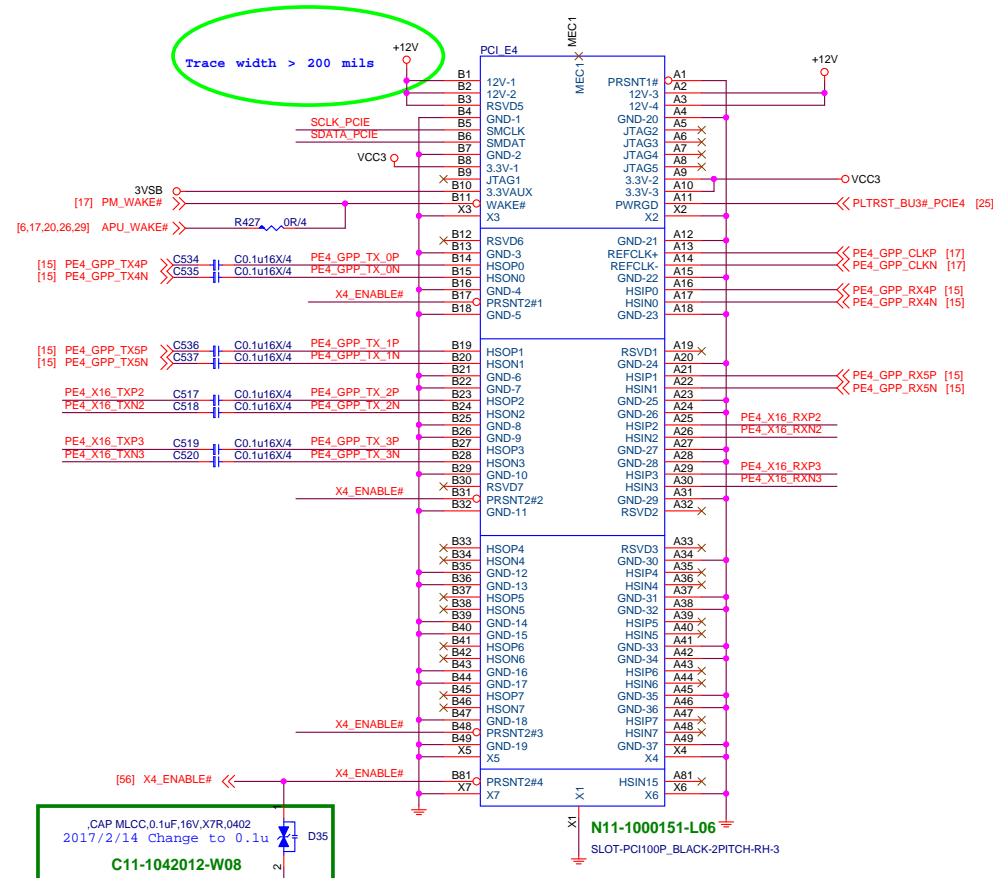
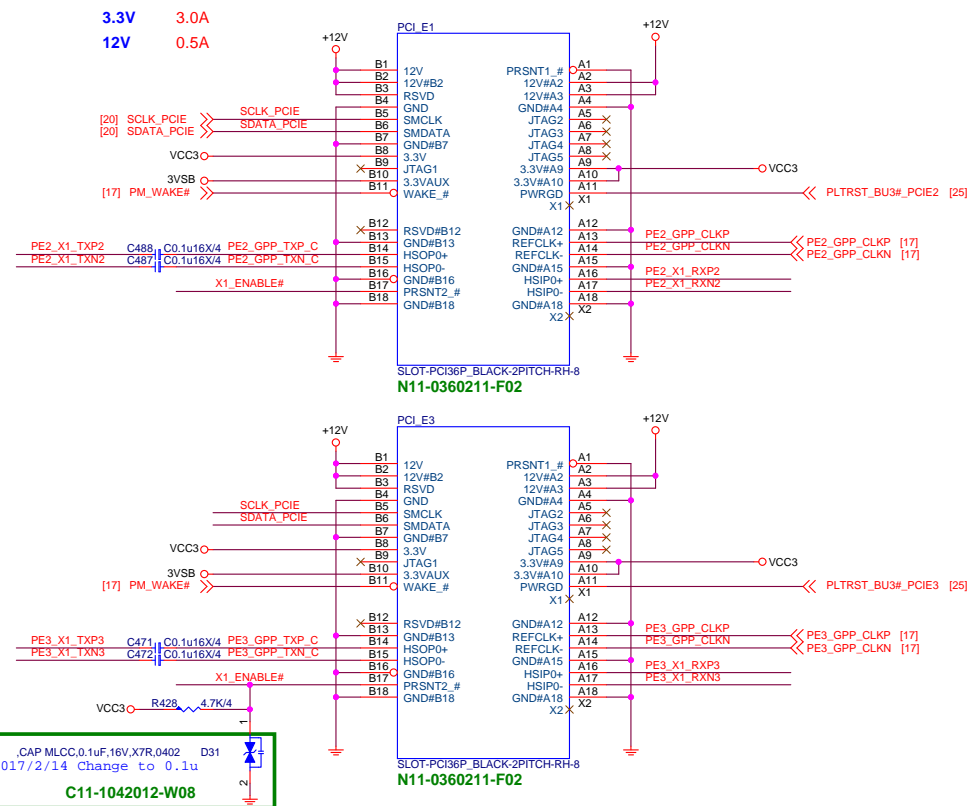
Vinafix.com



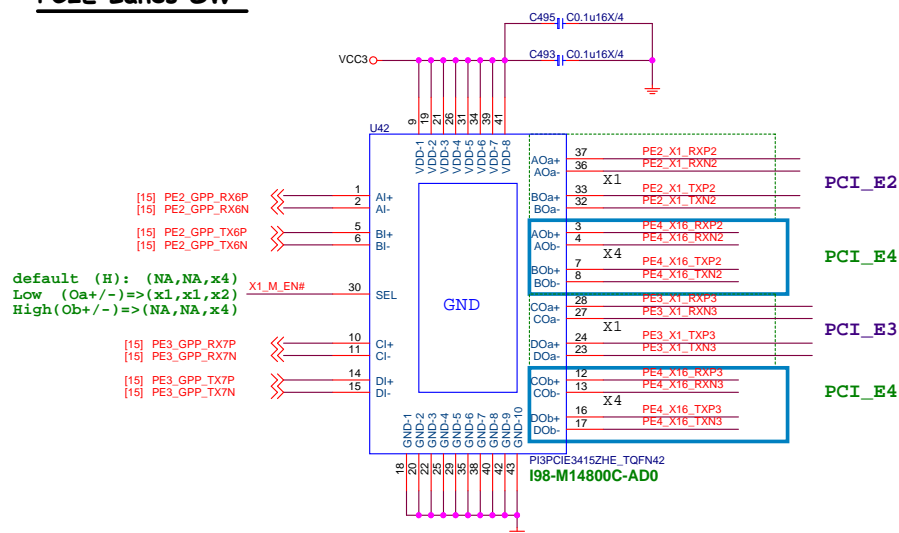
PCI Express x16 Slot

+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

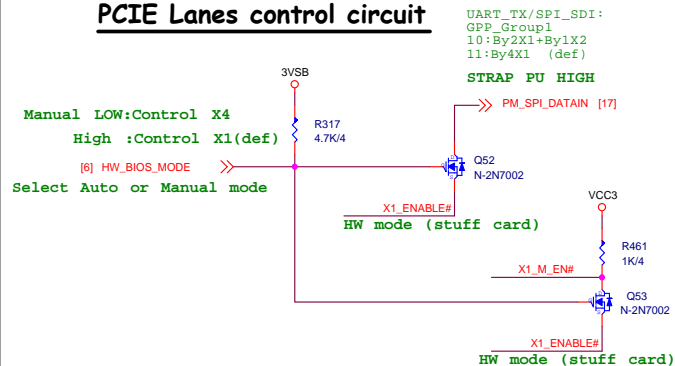
```
PCIE_X1 12V 0.5A
3.3V weak 375mA
```



PCIE Lanes SW



PCIE Lanes control circuit



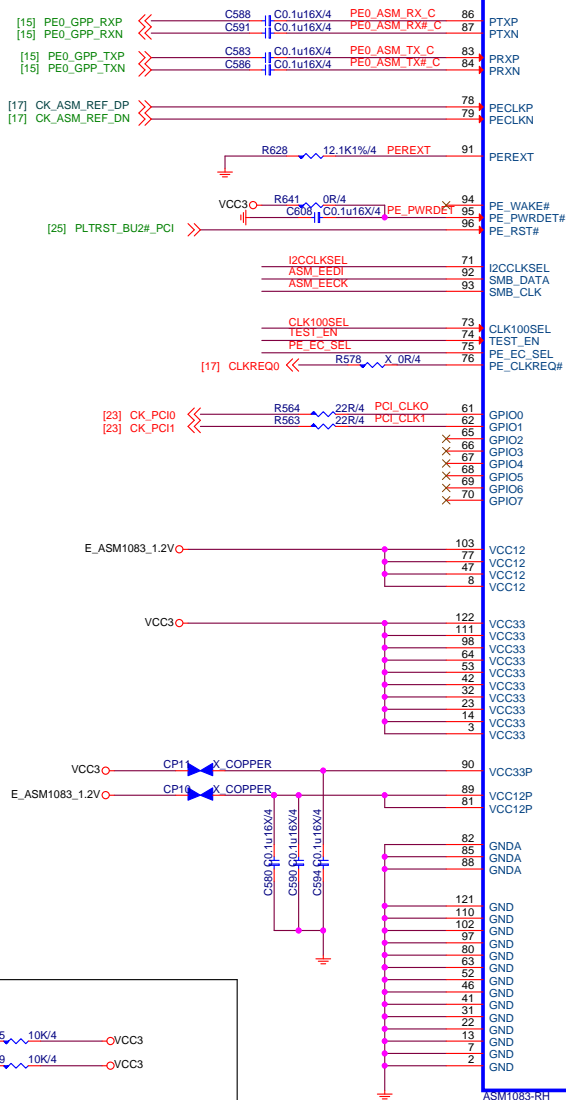
	HW_BIOS_MODE	Q52	Q53		X1_ENABLE#	PM_SPI_DATAIN
Manual x4	L	OFF	OFF		X	11:By4X1 (def)
Manual x1,x1,x2	H	ON	ON		L (Stuff PCIE_1)	10:By2X1+By1X2
HW x4	H	ON	ON		H	11:By4X1 (def)

PCI Express x4 Slot *1

+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA
PCI Express x1 Slot *2		
+12V		- 1 A
+VCC3		- 6A
+3V3_S5	(wake)	- 750mA
+3V3_S5	(no wake)	- 40mA



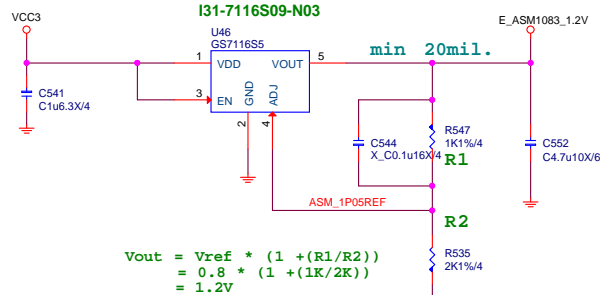
Title		21 PCIE X1/PCIE X4	
Size	Document Number	Rev	
Custom	MS-7A34	20_30_05S	
Date:	Tuesday, June 20, 2017	Sheet	21 of 60



ASM1083

ASM1083-RH
B0D-0108314-AD0

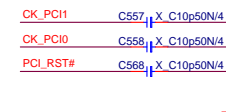
ASM_EECK R635 10K/4 VCC3
ASM_EEDI R629 10K/4 VCC3



$$V_{out} = V_{ref} * (1 + (R1/R2)) = 0.8 * (1 + (1K/2K)) = 1.2V$$

1.2V@115mA

EMI



H/W Strapping

PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

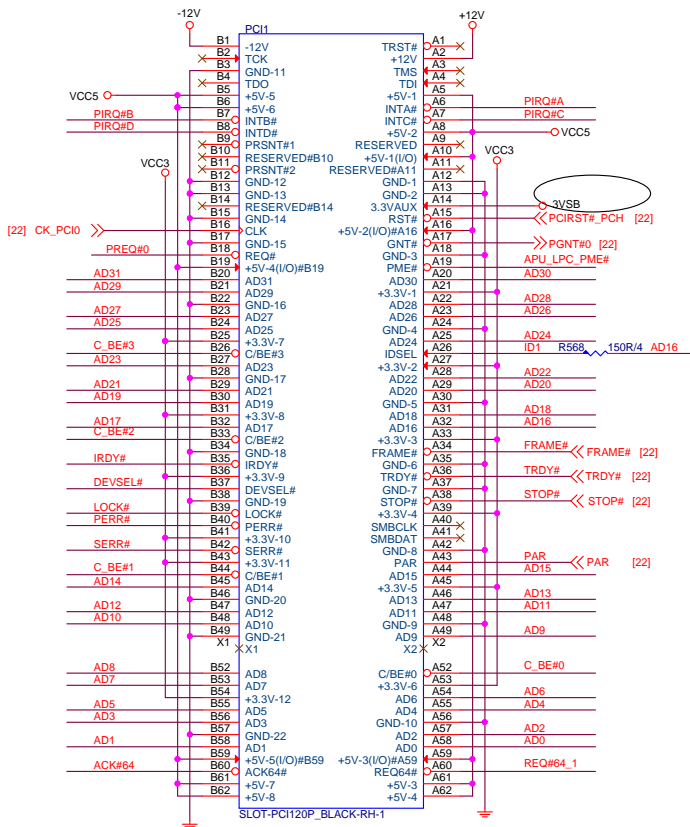
I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK



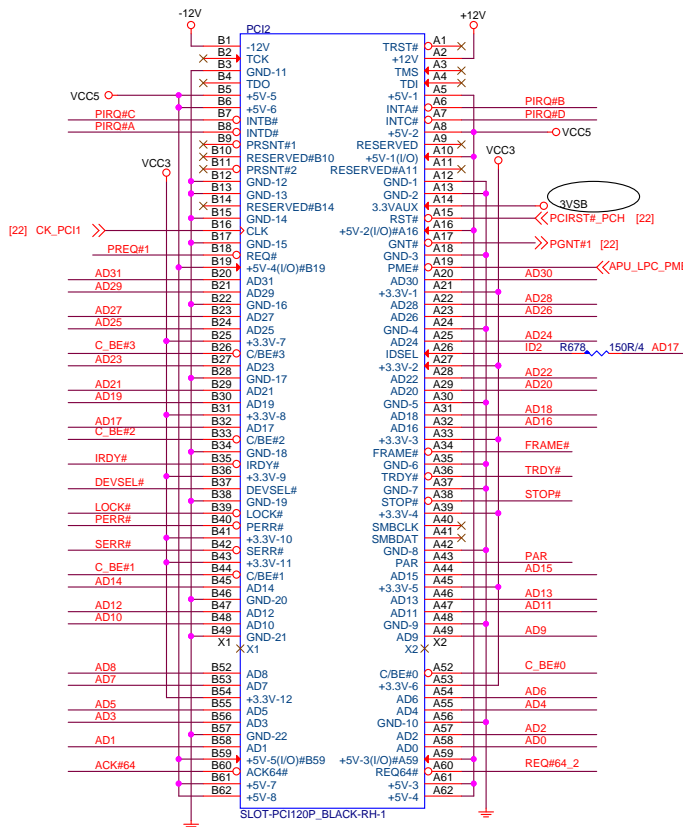
MICRO-STAR INT'L CO.,LTD

MS-7A34

Size	Document	Description	Rev
Custom	ASM1083	PCI Br.	20_30
Date: Tuesday, June 20, 2017	Sheet	22	of 60



N11-1200541-C67
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

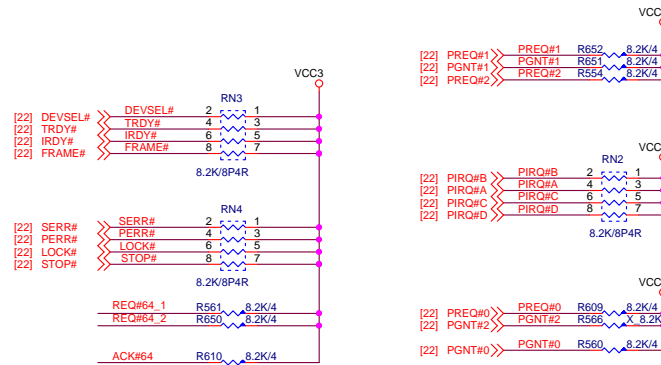
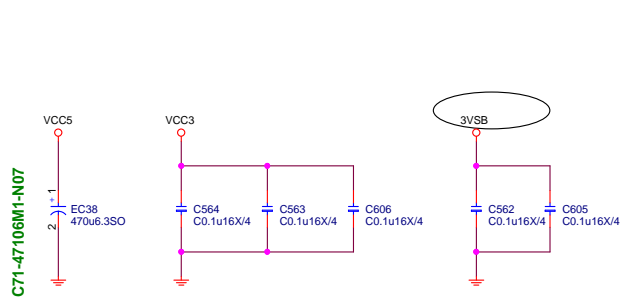


N11-1200541-C67
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

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AD31_0] <<< AD31_0] [22]
 C_BE#3_0] <<< C_BE#3_0] [22]

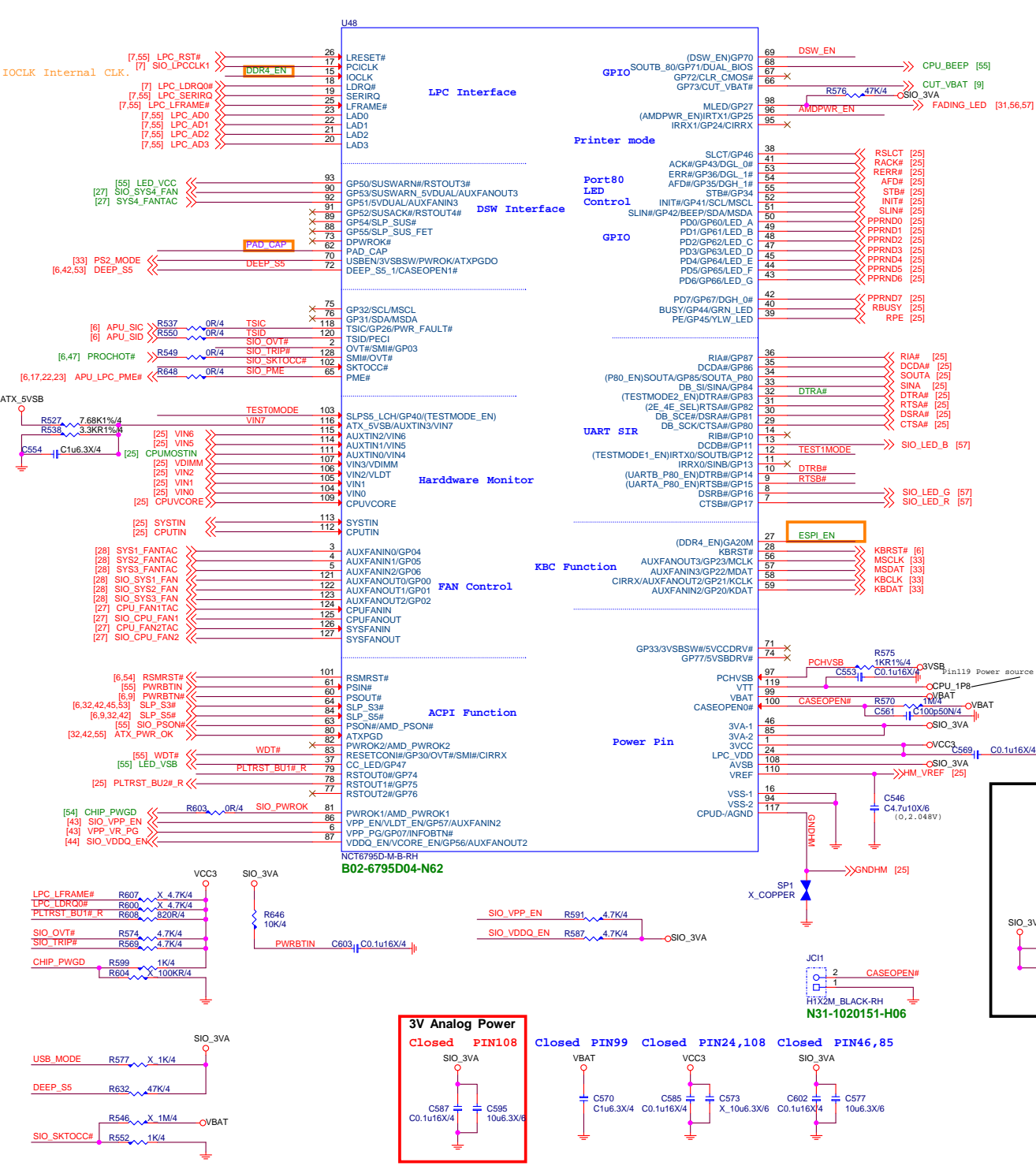
PCI PULL-UP / DOWN RESISTORS



PCI Slot *2	
+12V	- 1 A
+VCC3	- 15.2A
+VCC5	- 10A
+3V3_S5	(wake) - 750mA
+3V3_S5	(no wake) - 40mA



MICRO-STAR INT'L CO.,LTD			
MS-7A34			
Size	Document	Description	Rev
Custom	PCI Slot		20_05
Date: Tuesday, June 20, 2017	Sheet	23	of 60



DSW_EN R639 X 0R/4

AMDPWR_EN R582 X 0R/4

USB_MODE [32]

POWER ON STRAPPING PIN FOR NCT6793/6795

PIN	6793/6795	NAME	Circuit	NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE	ENABLE	UARTA80	ENABLE	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE	ENABLE	UARTB80	ENABLE	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE	ENABLE	TEST1MODE	TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable			
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable			
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E			LRESET
32	6793 TESTMODE2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%			INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80			LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW			INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ			INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE			INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

Co-Lay NCT6795 (PIN9) (RTSB#) 80_ENA 0=Disable 1=Enable (PIN10) (DTRB#) 80_ENB 0=Disable 1=Enable (PIN32) (DTRA#) FANOUT 0=50% 1=100% (PIN12) TEST_MODE_EN1 0=Disable 1=Enable (PIN103) TEST_MODE_EN0 0=Disable 1=Enable (PIN27) ESPI_EN0 0=LPC 1=ESPI (PIN15) DDR4_EN 0=Disable 1=Enable

SIO_3VA

VCC3

R615 X 1K/4

ESPI_EN

R616 1K/4

SIO_3VA

R579 X 1K/4

RTSB#

R586 680R/4

R585 X 1K/4

DTRB#

R589 680R/4

R637 1K/4

DTRA#

R631 X 680R/4

TEST1MODE

R594 680R/4

TESTMODE

R551 680R/4

3V Analog Power

Closed PIN108

C587 C0.1u16X/4

C595 10u6.3X/6

C570 C1u6.3X/4

C585 C0.1u16X/4

C573 X 10u6.3X/6

C602 C0.1u16X/4

C577 10u6.3X/6

Closed PIN99

Closed PIN24,108

Closed PIN46,85

VCC3

SIO_3VA

VBAT

C570 C1u6.3X/4

C585 C0.1u16X/4

C573 X 10u6.3X/6

C602 C0.1u16X/4

C577 10u6.3X/6

MSI

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MICRO-START INTL CO.,LTD.

SIO NCT6795D

Size Custom

Document Number MS-7A34

Date: Tuesday, June 20, 2017

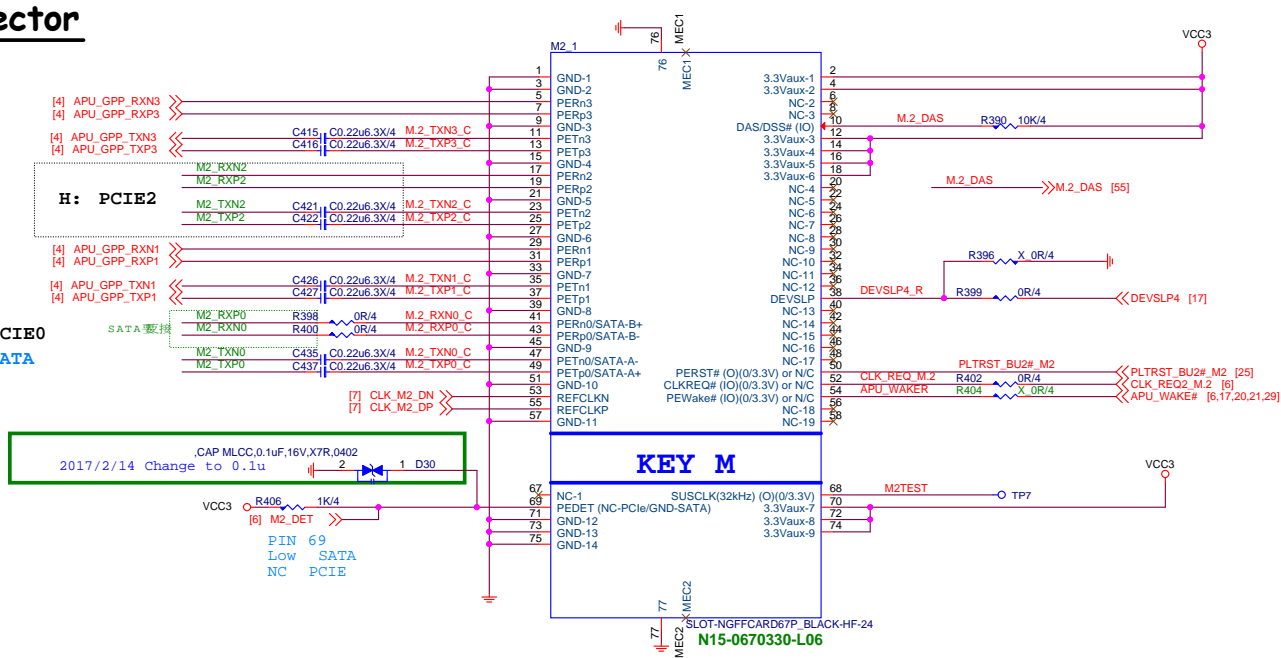
Sheet 24 of 60

Rev 20_30_05S

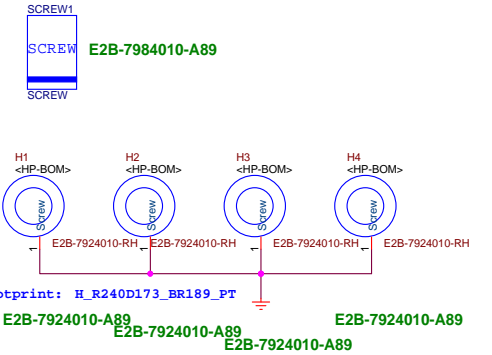
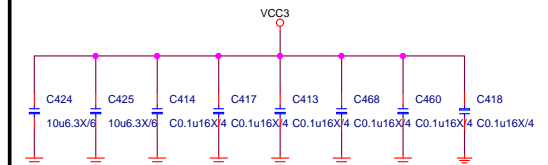
M.2 Connector

3.3V@2.5A

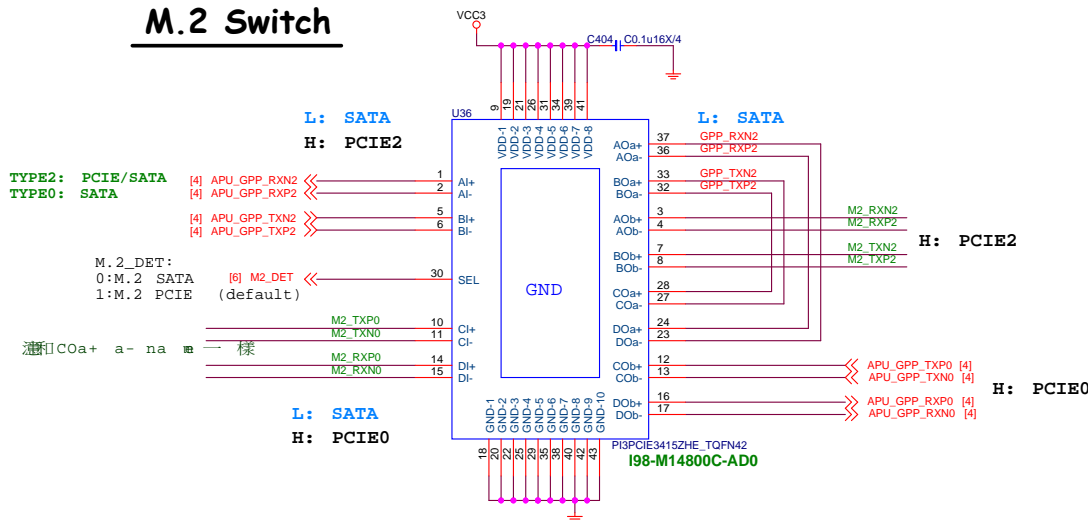
H: PCIE0
L: SATA



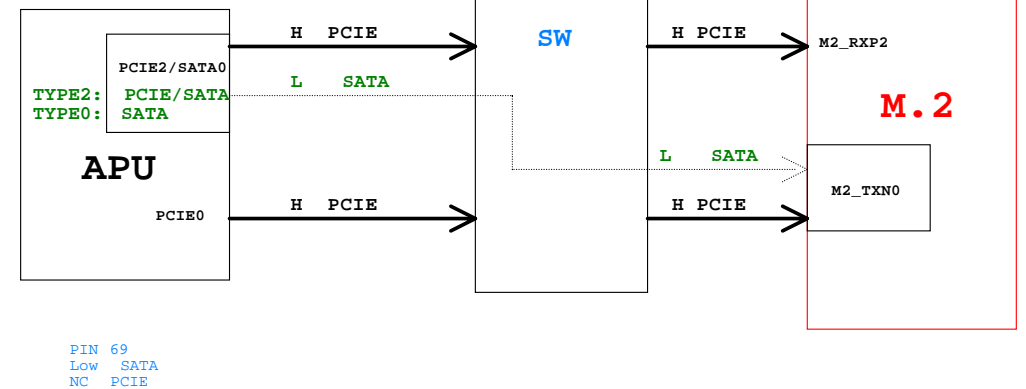
3.3V@2.5A



M.2 Switch



HW Default
M.2 Insert



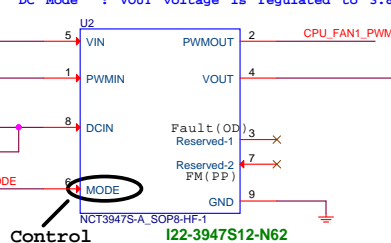
SW:
H:M.2 PCIE
L:M.2 SATA

CPUFAN

TYPE K : 4 PIN FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

GPIO 自由切换 PW M/DC

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8*DCIN voltage.



From SIO

[24] SIO_CPU_FAN1

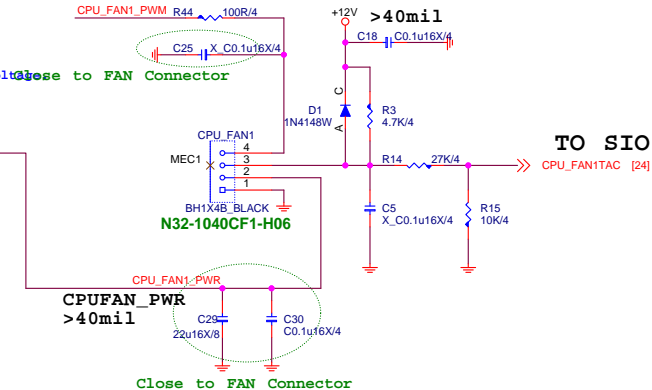
FIX MODE unstuff

	MODE(PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Internall pull up 1.65V

GPIO Control

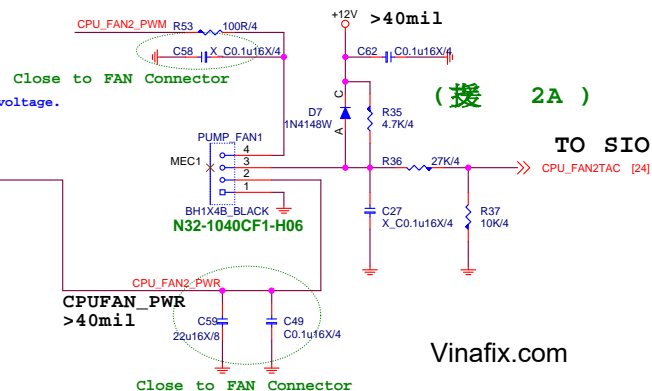
I22-3947S12-N62



TO SIO

CPU_FAN1TAC [24]

Close to FAN Connector



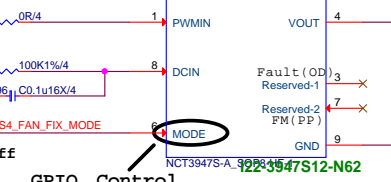
Vinafix.com

Close to FAN Connector

SYSFAN

C3 Close to U1 PIN5

PWM Mode : VOUT voltage follows VIN voltage
DC Mode : VOUT voltage is regulated to 3.8*DCIN voltage.



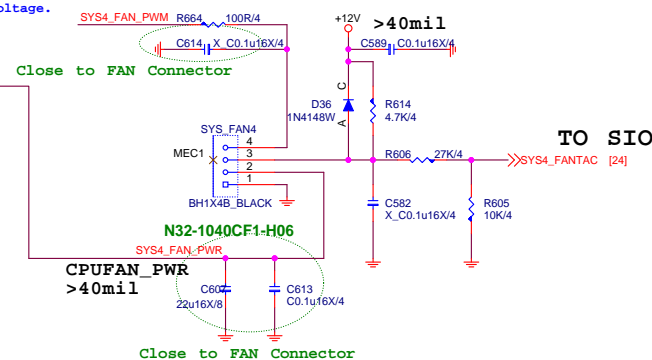
From SIO

[24] SIO_SYS4_FAN

FIX MODE unstuff

GPIO Control

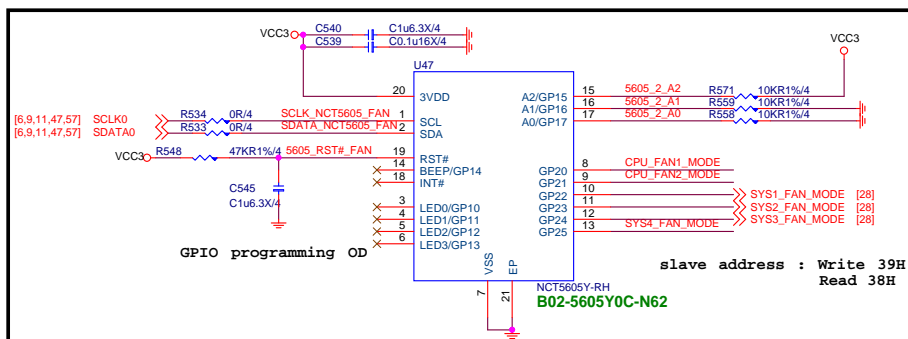
I22-3947S12-N62



TO SIO

SYS4_FANTAC [24]

Close to FAN Connector



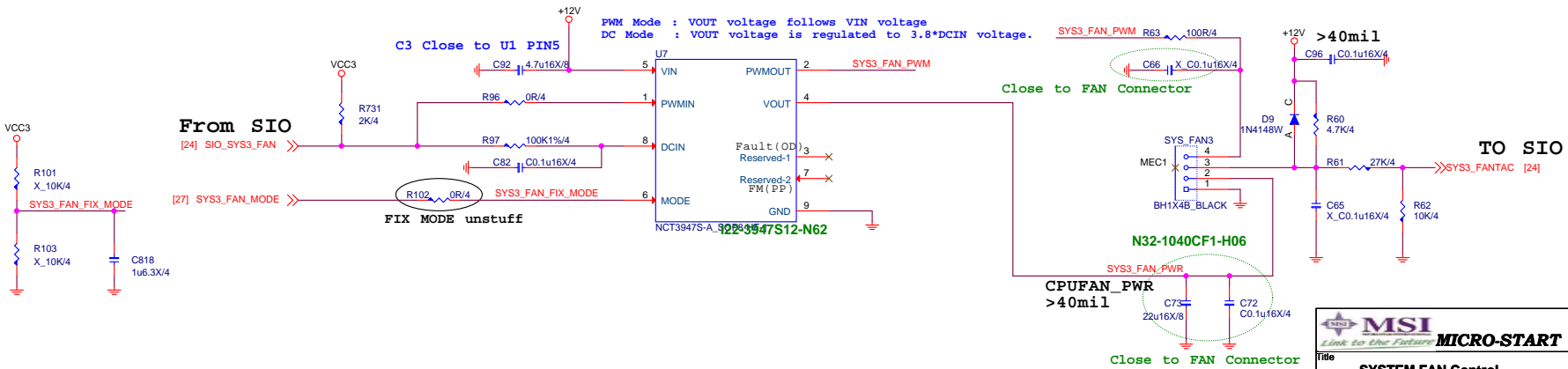
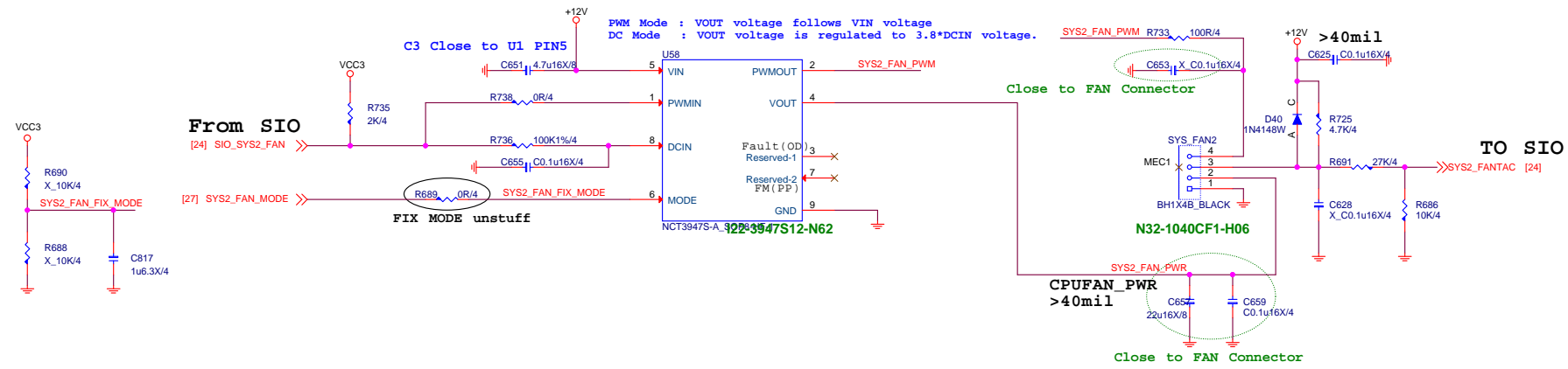
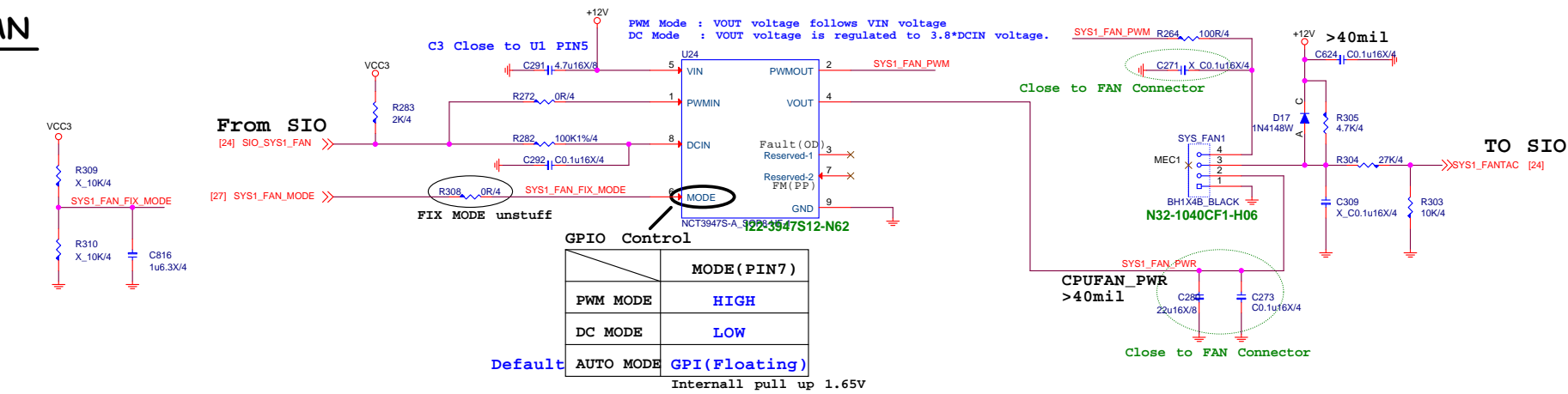
slave address : Write 39H

Read 38H

Link to the Future		
MICRO-START INTL CO.,LTD.		
Title CPU FAN Control		
Size Custom	Document Number MS-7A34	Rev 20_30_05S
Date: Tuesday, June 20, 2017	Sheet 27 of 60	

Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

SYSFAN



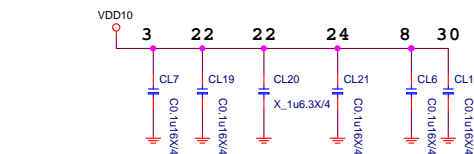
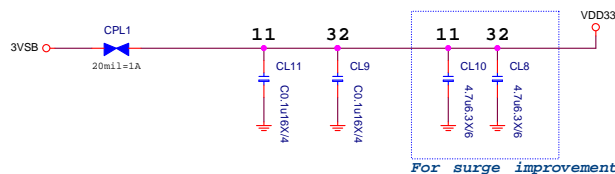
Title			
SYSTEM FAN Control			
Size	Document Number		Rev
Custom	MS-7A34		20_30
Date:	Tuesday, June 20, 2017	Sheet 28 of 60	

RTL8111H Giga LAN

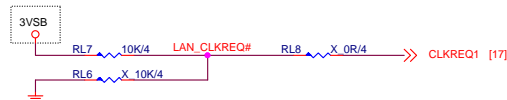
3.3V@177.57mA



Remove pull-up R if R existence on motherboard (or SB has internal pull-up R).

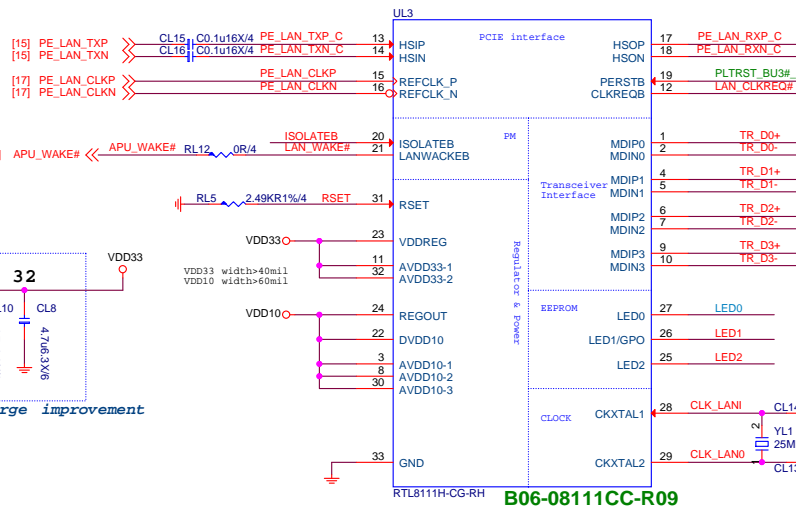


Pull-up resistor RL9 required to either 3.3V suspend or core rail depending on the power well of the PCH input CLKREQ# buffer.



8111H POWER Consumption

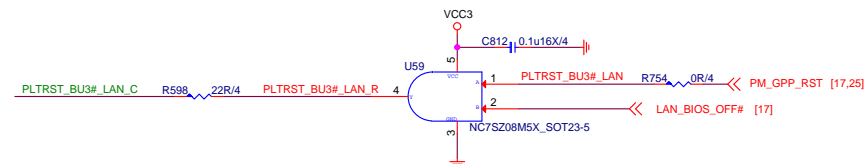
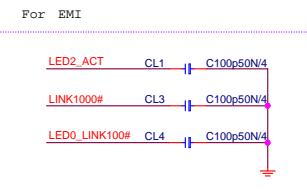
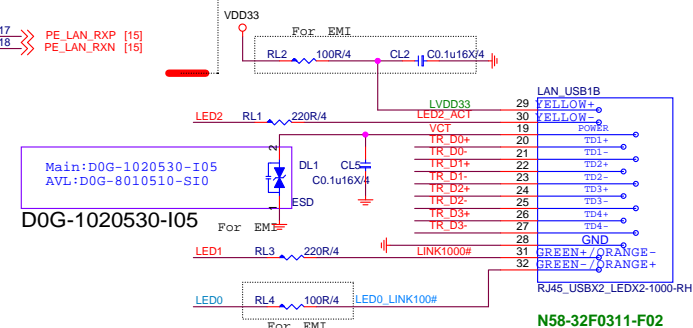
	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



Pin33: 4 via from top layer to GND layer and make the via at the center of IC.

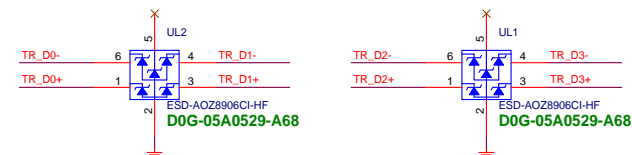
PIN19:
AMD platform connect to PCIE_RST#,
don't connect to A-RST#.
INTEL platform connect to PLT_RST#.

LAN Connector



ESD Protect

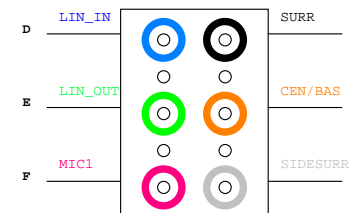
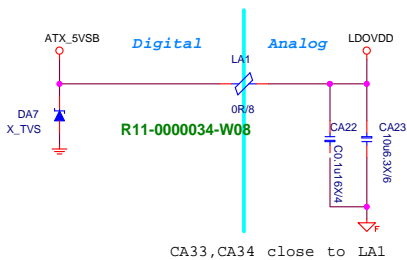
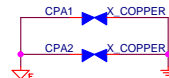
D0G-0200529-A68
D0G-0100619-I05

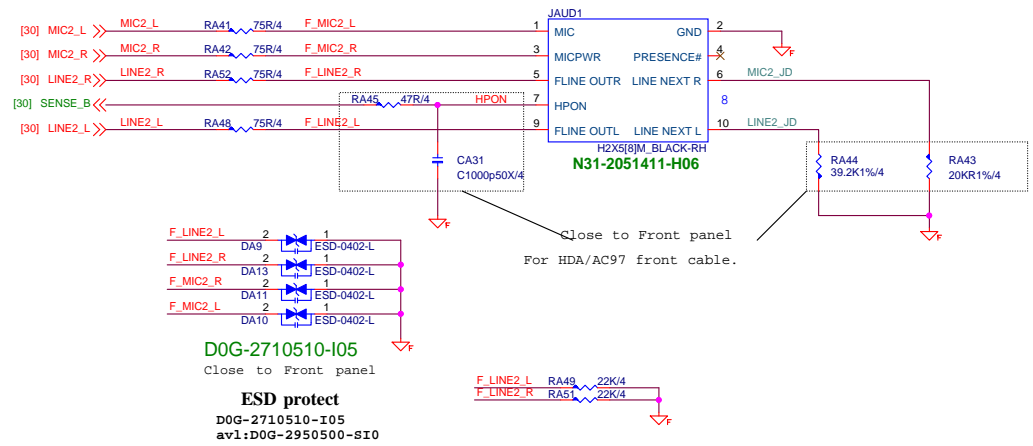
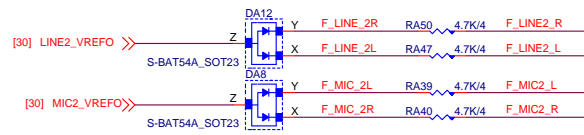


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MICRO-START INTL CO.,LTD.

Title LAN-8111H		
Size Custom	Document Number MS-7A34	Rev 20_30_05S
Date: Tuesday, June 20, 2017	Sheet 29	of 60

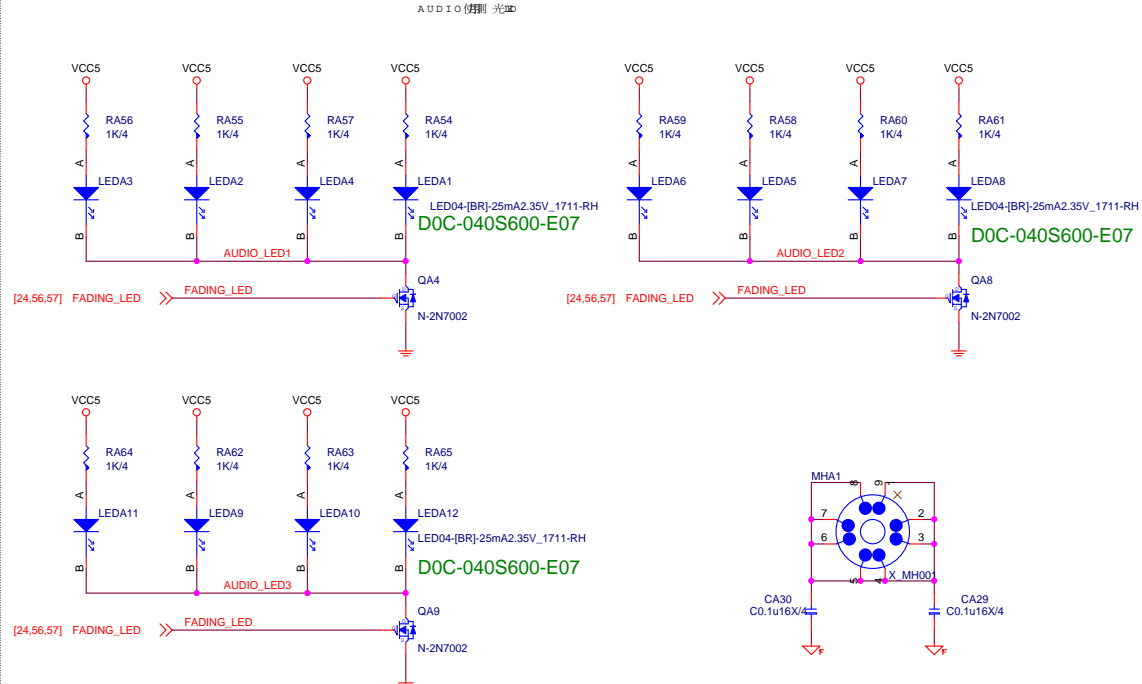
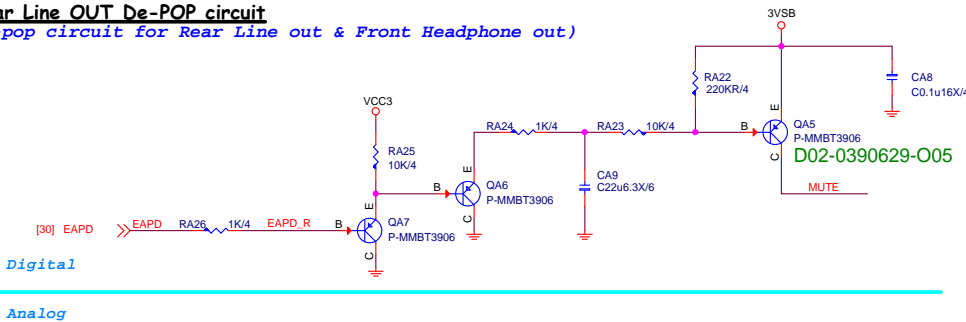
Follow APU power well



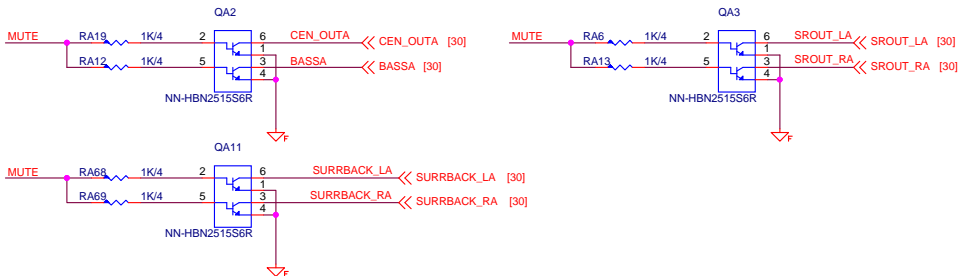


Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)

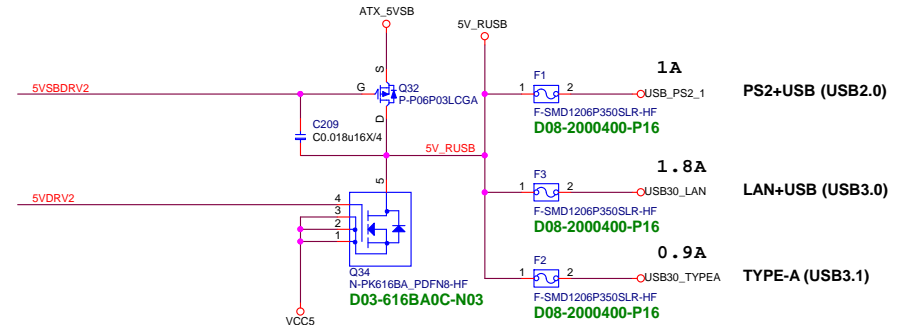
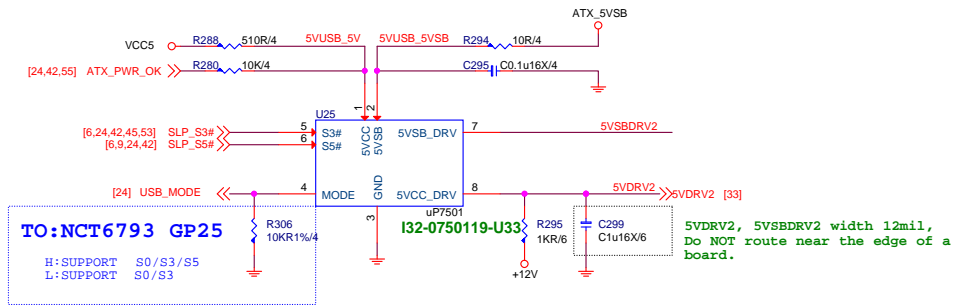


(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA6, CA7, CA9,to TVS)



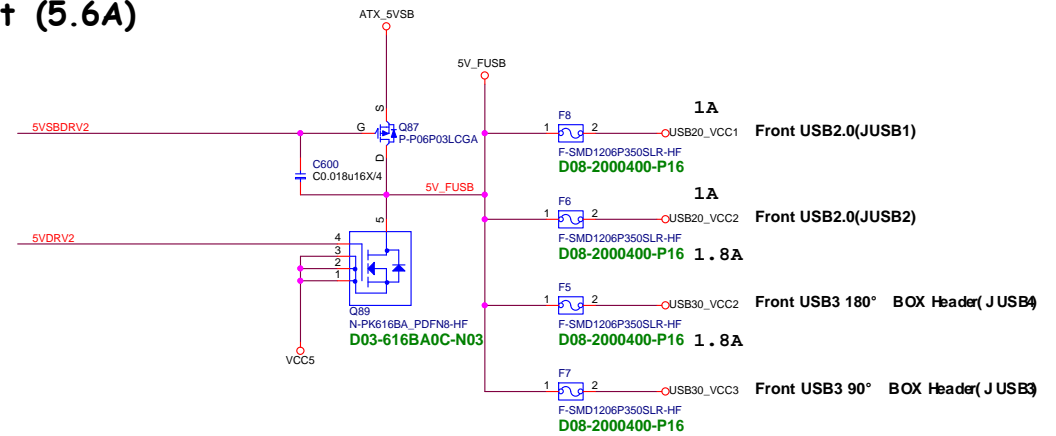
Title		Audio ALC892	
Size	Document Number	Rev	
Custom	MS-7A34	20_30_05S	
Date:	Tuesday, June 20, 2017	Sheet	31 of 60

USB Power



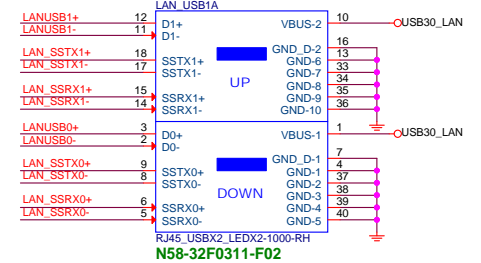
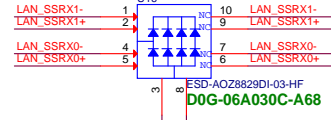
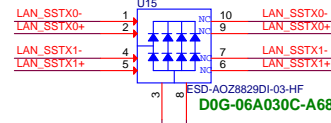
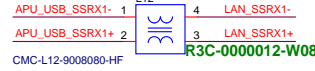
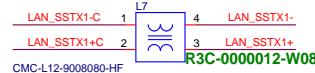
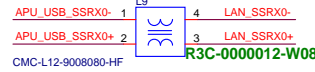
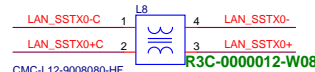
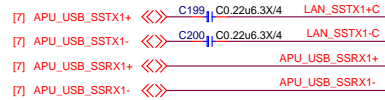
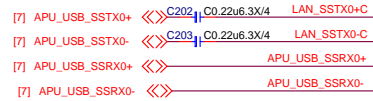
Rear (3.7A)

Front (5.6A)

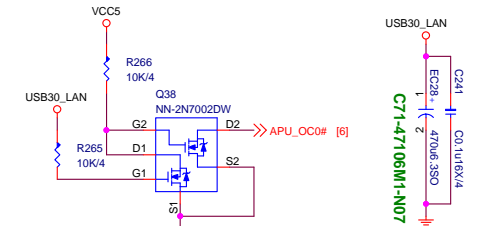
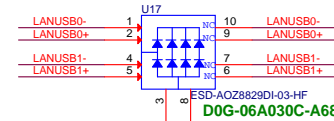
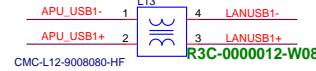
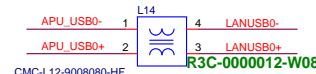
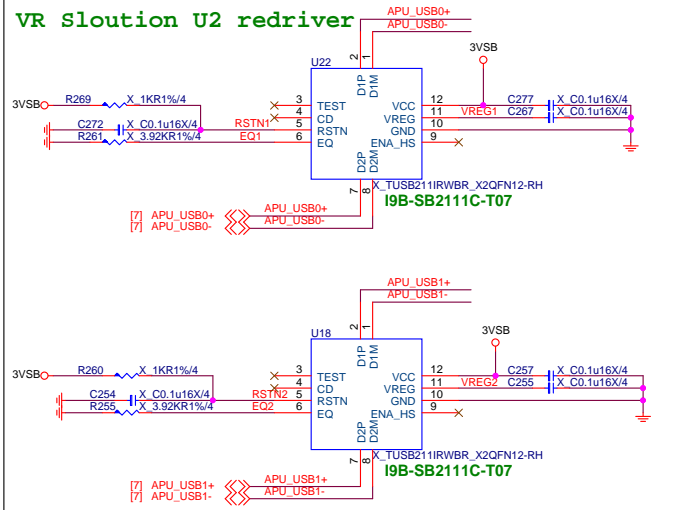


LAN+USB (USB3.0)

5V@1A
VR Sloution U2 redriver

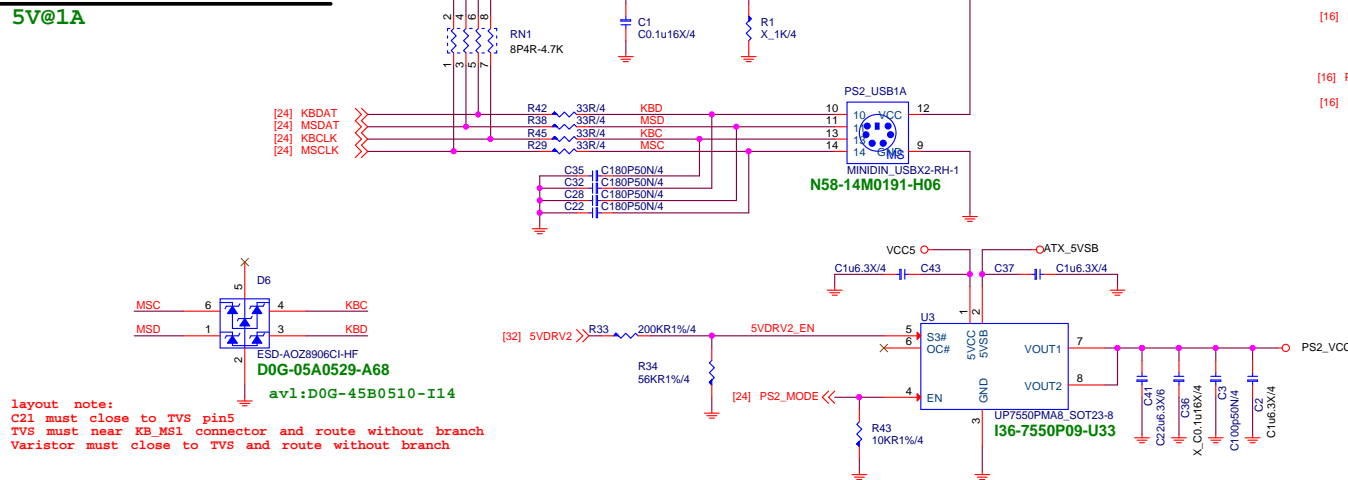


VR Sloution U2 redriver



PS2+USB (USB2.0)

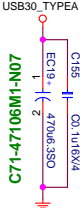
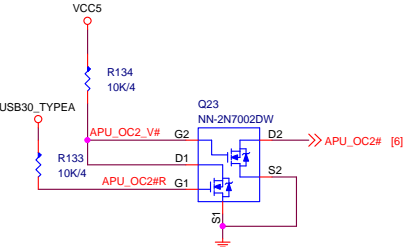
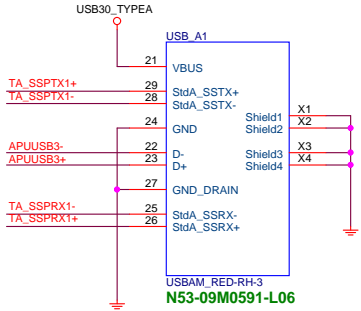
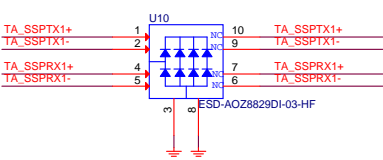
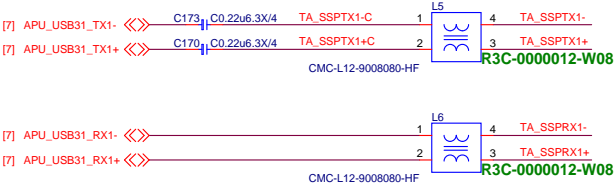
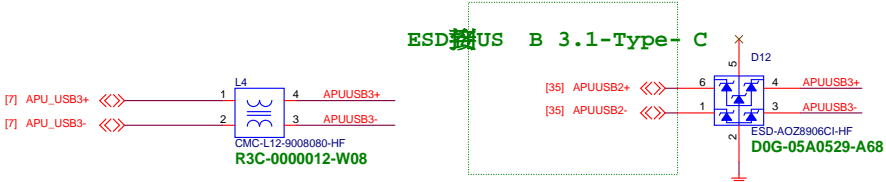
5V@1A



TYPE-A (USB3.1)

5V@0.9A

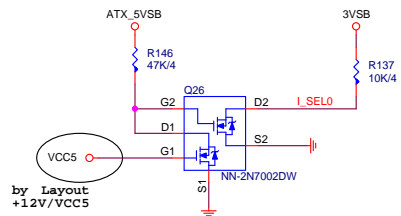
Vinafix.com



USB 3.1-Type-C

5V@3A

Current Mode

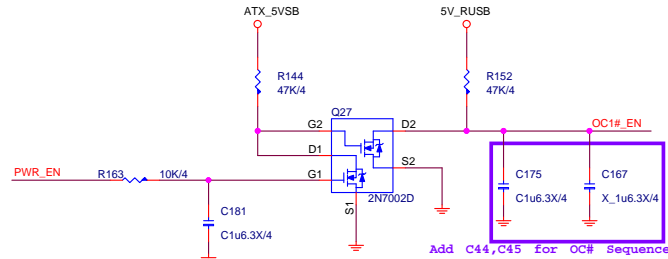


by Layout +12V/VCC5

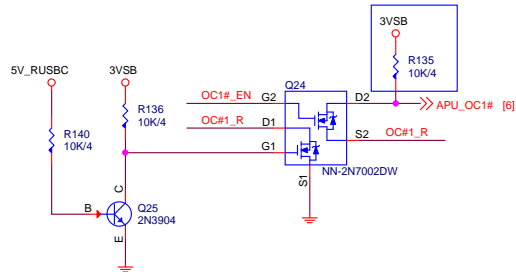
I_SELO : I_SEL1	
X 0	Default for 900mA
U 1	1.5A @5V
1 1	3A @5V

1.5A under S3 mode
3A under S0 mode

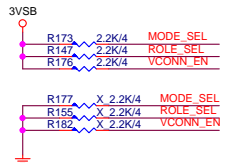
VBUS OC#



No need pull up if 3vsub at PCH Side



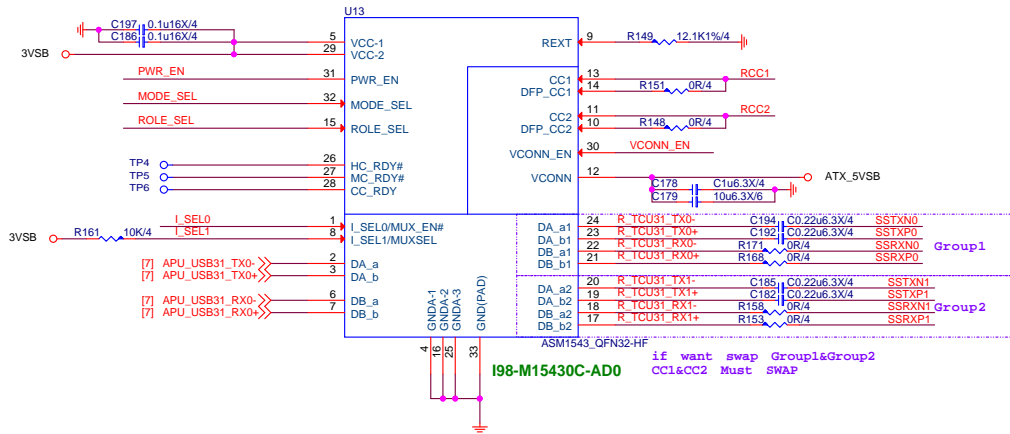
ASM1543 MUX



MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

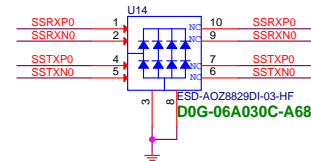
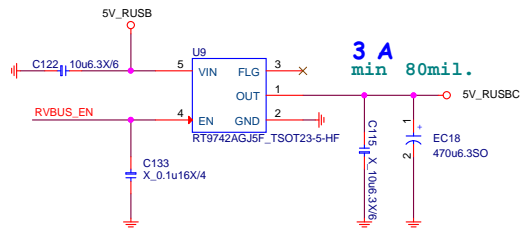
VCONN_EN	
1	enable
0	disable



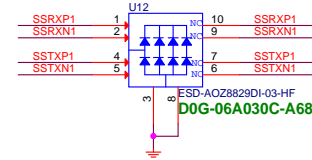
if want swap Group1&Group2
CCL&CC2 Must SWAP

198-M15430C-AD0

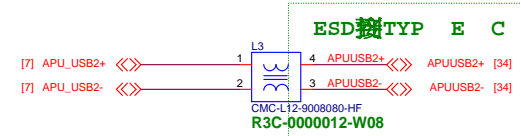
3 A min 80mil.



D0G-06A030C-A68

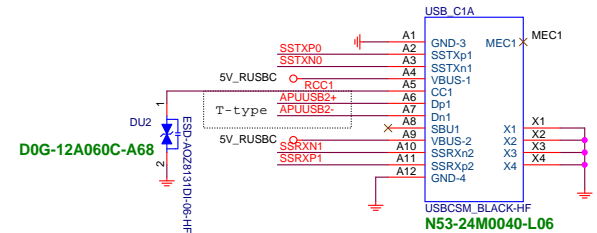


D0G-06A030C-A68

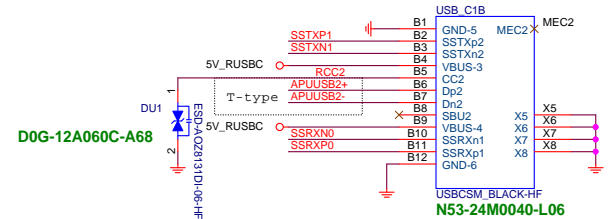


ESD-TYPE C

CMC-L12-9008080-HF
R3C-0000012-W08



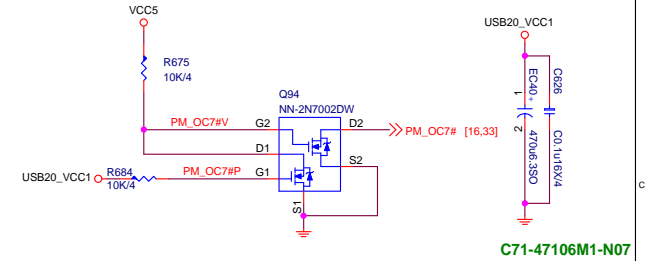
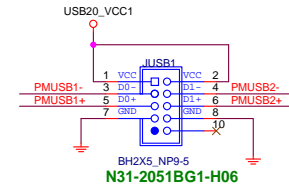
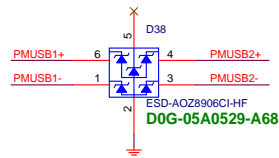
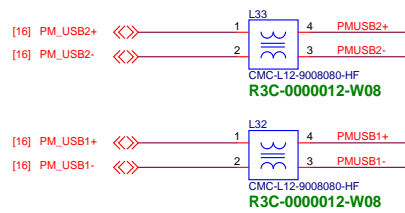
D0G-12A060C-A68



D0G-12A060C-A68

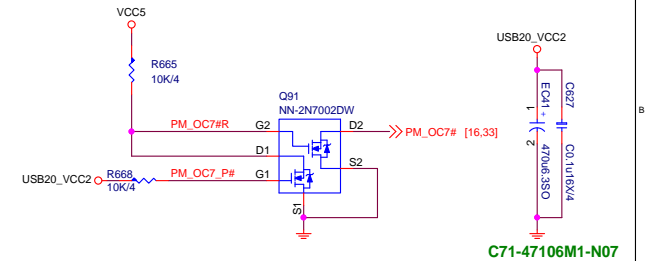
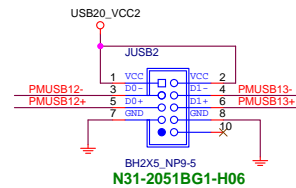
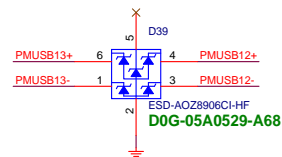
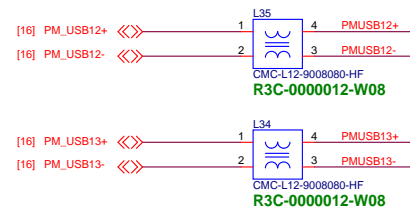
Front USB2.0(JUSB1)

5V@1A

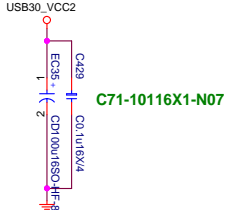
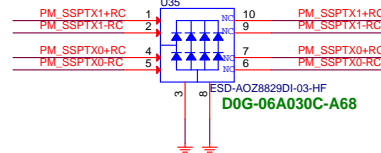
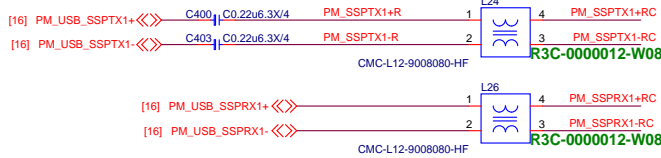
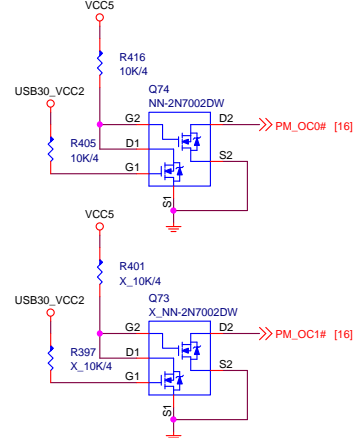
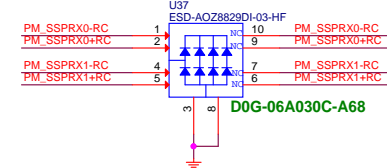
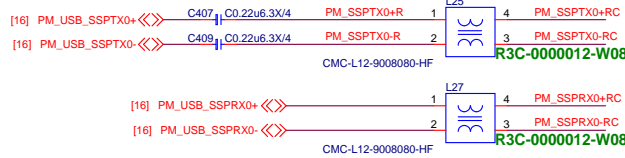
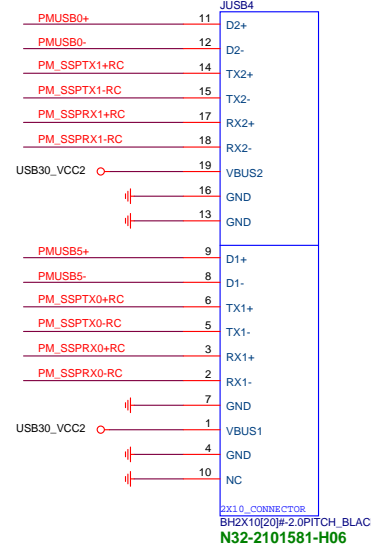
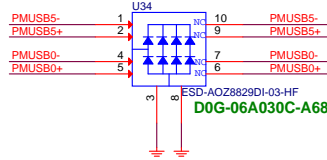
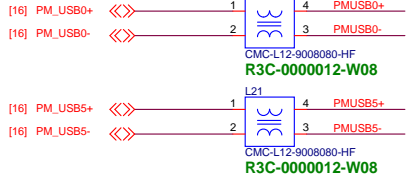


Front USB2.0(JUSB2)

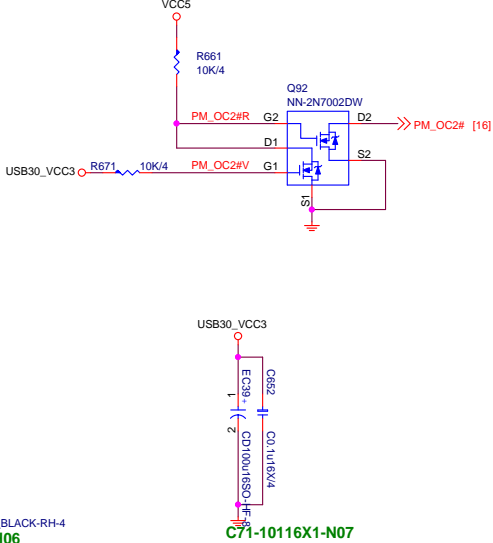
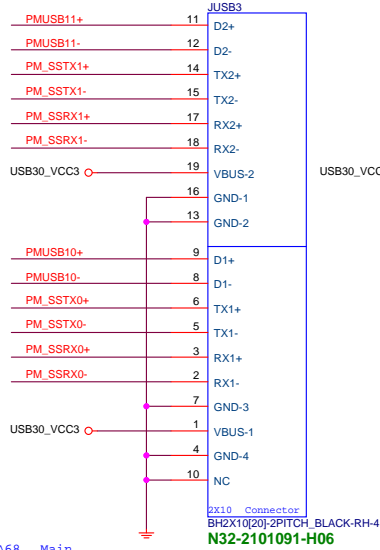
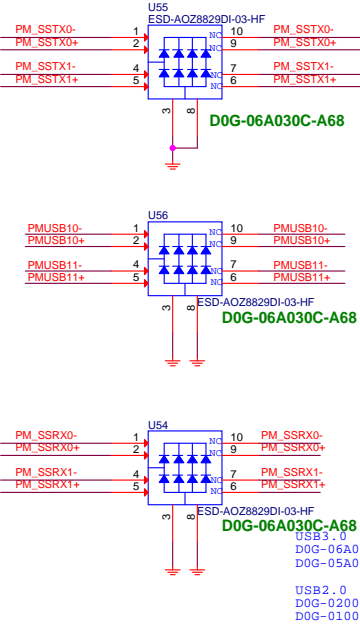
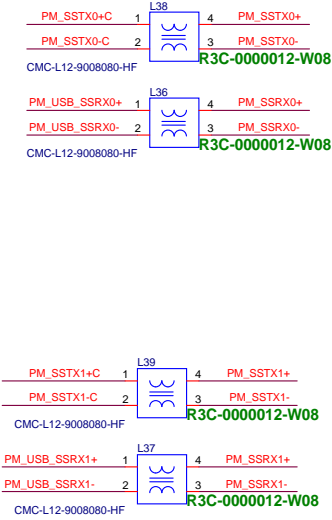
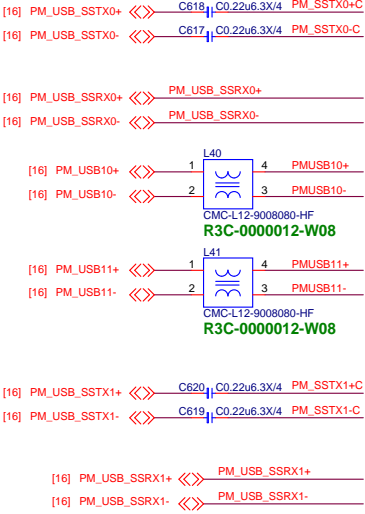
5V@1A



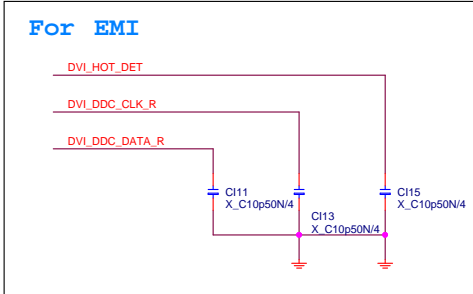
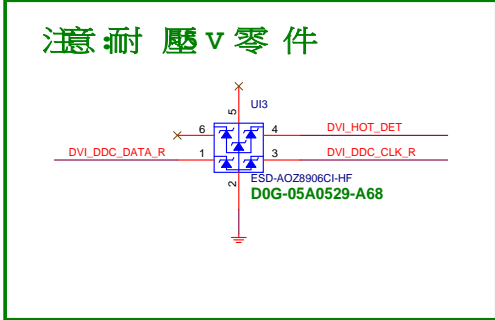
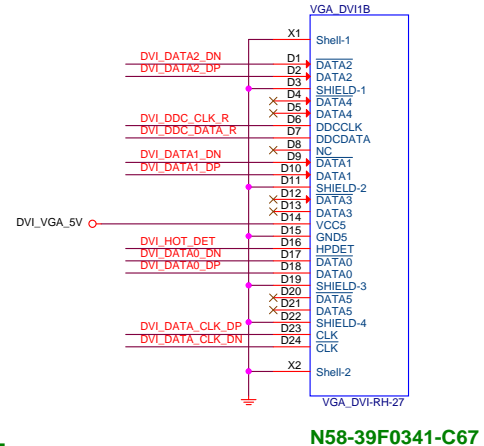
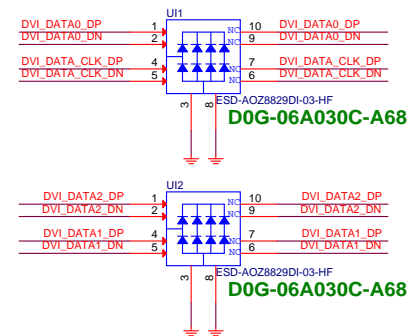
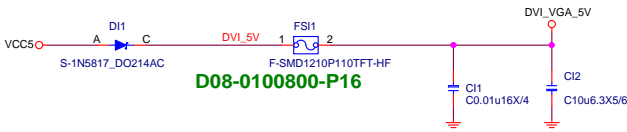
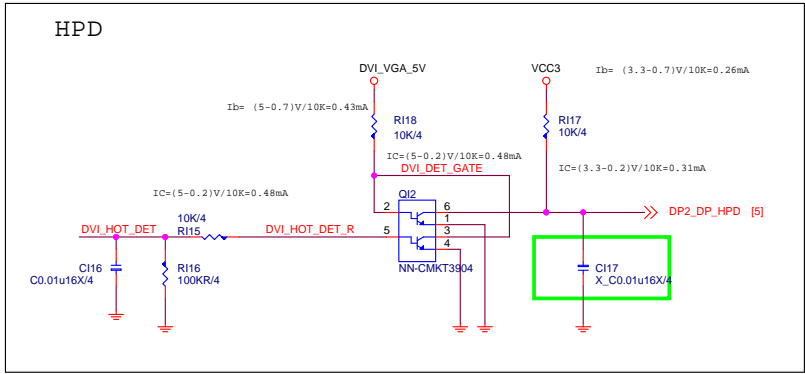
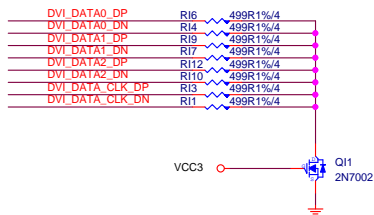
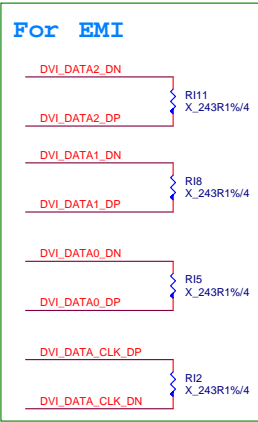
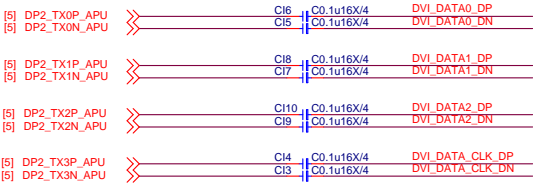
5V@1.8A



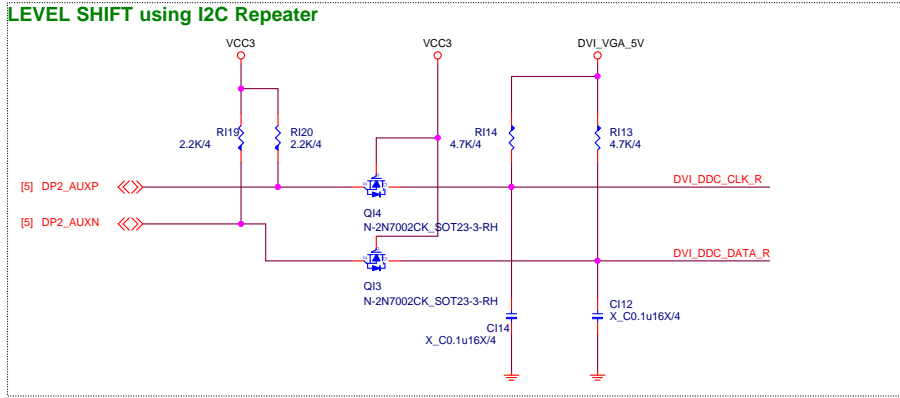
Front USB3 180° BOX Header(J USB3)
5V@1.8A



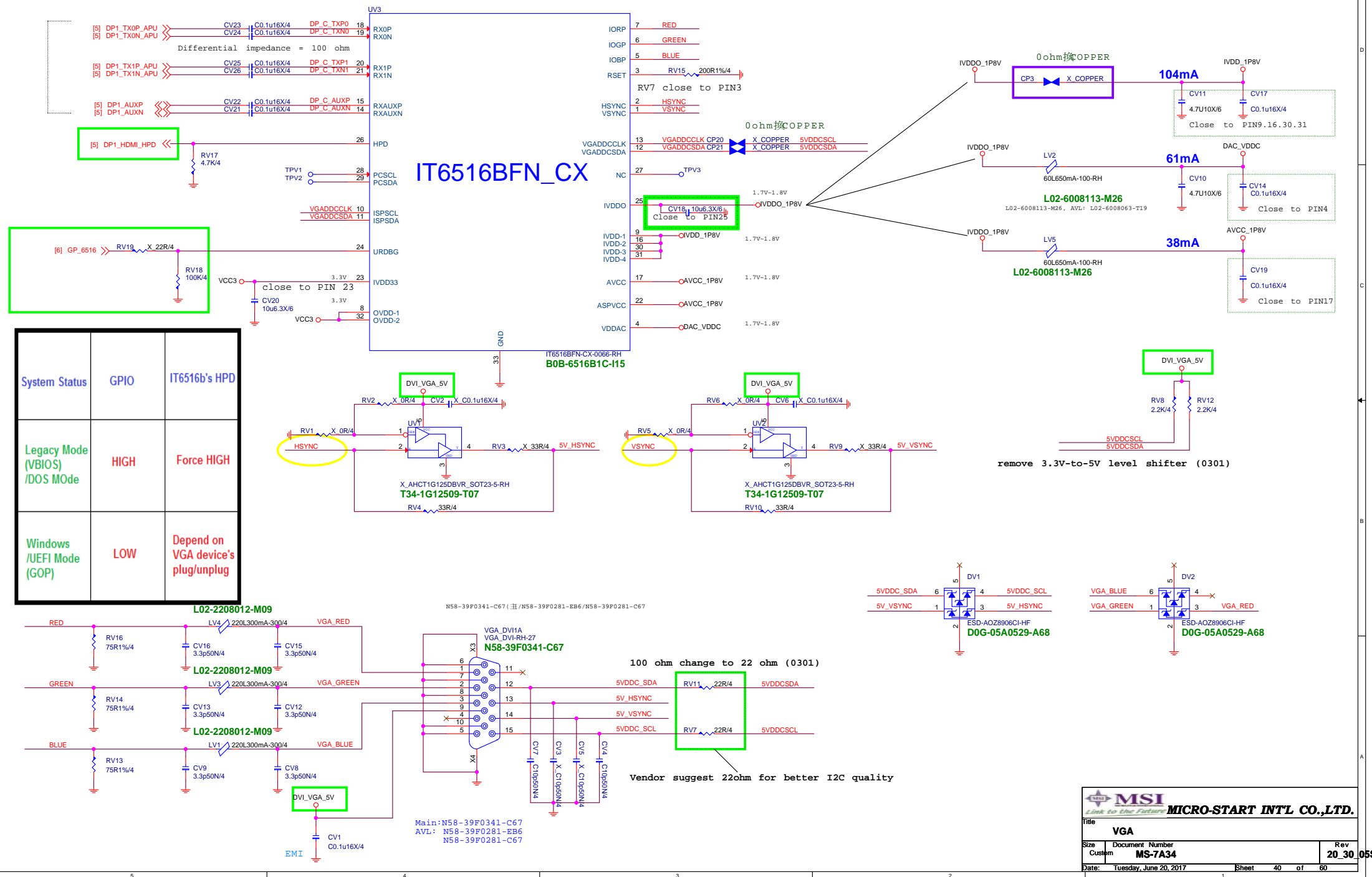
DVI CONNECTOR



Vinafix.com

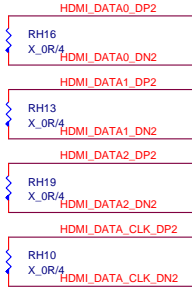
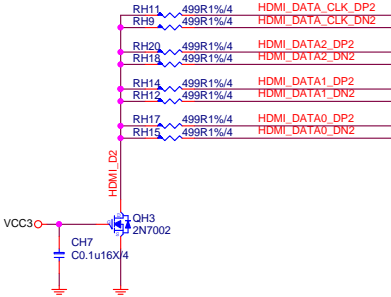
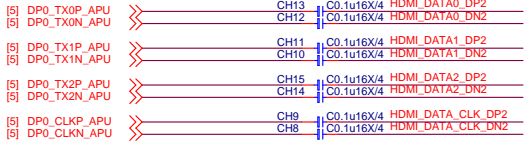


Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining

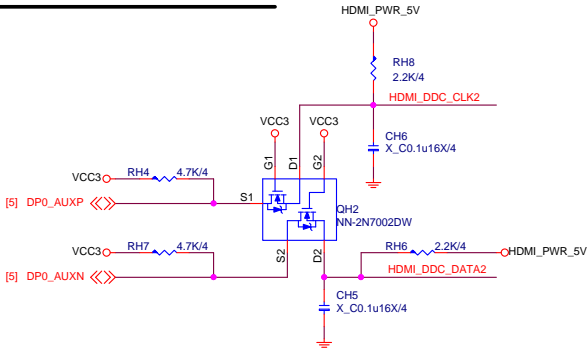


HDMI CONNECTOR

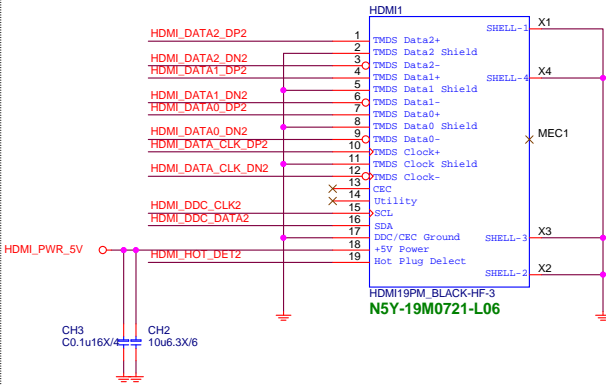
For HDMI 1.4



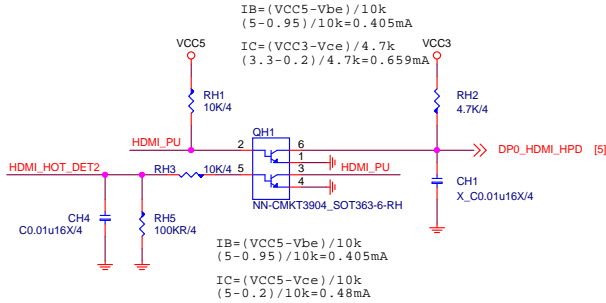
AUX Level Shifter



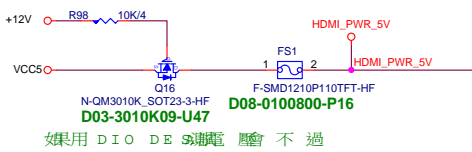
Connector



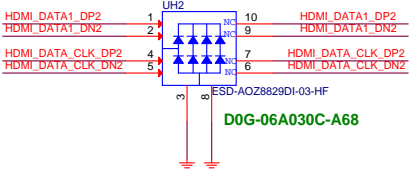
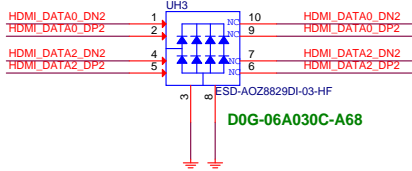
HPD Circuit



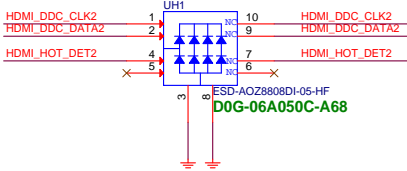
Connector Power



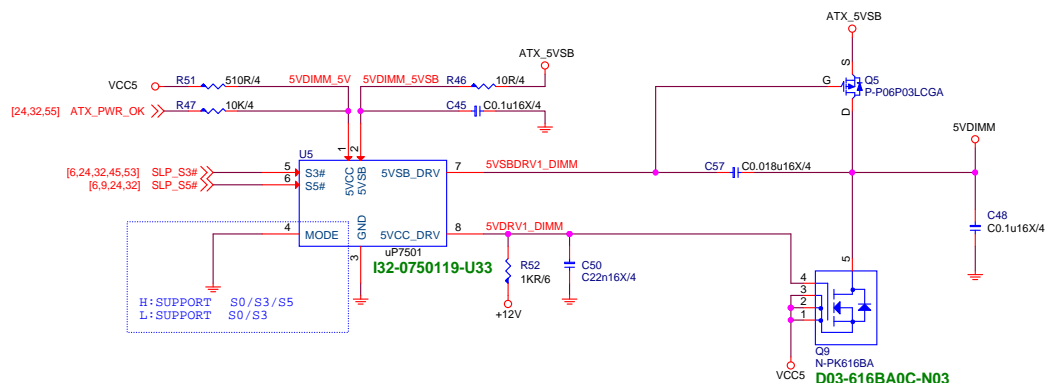
For EMI



注意耐壓v零件



5VDIMM FOR DDR



3VSB cost down

3.3V@2.63A

1.05V@0.05A

VDDBT_RTC G@4.5uA

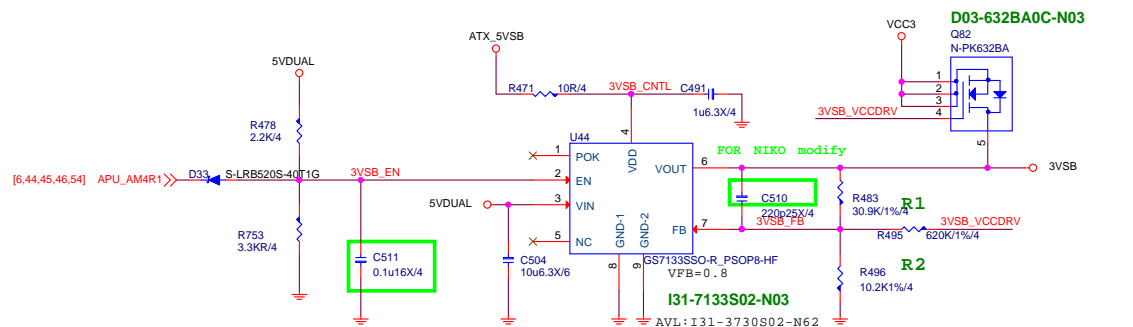
FCH@0.07A

CPU@0.25A

PCI @0.75A

PCIE*4 @1.5A

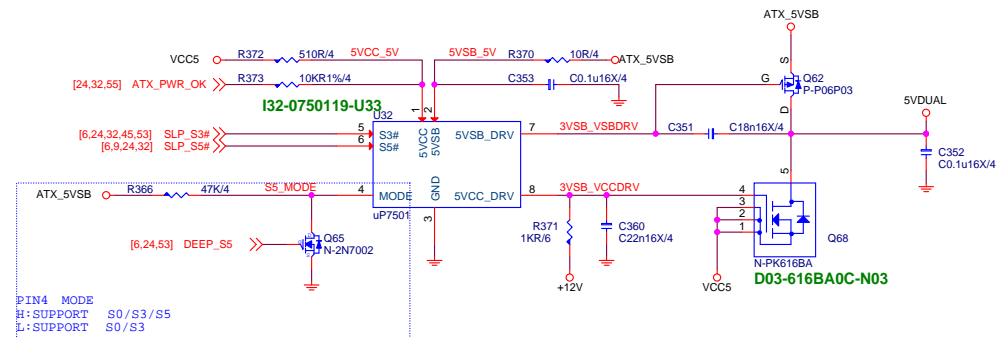
USB TYPE-C @0.9mA



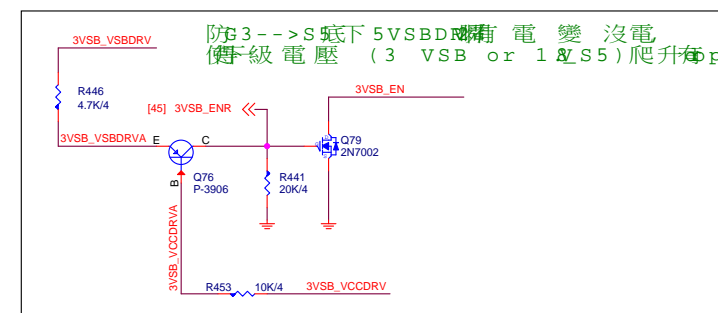
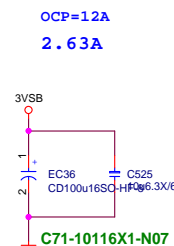
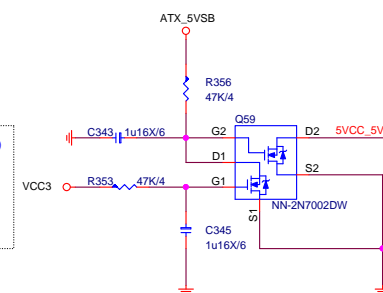
VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

5VDUAL For 3VSB, CPU 1.8V, VDD

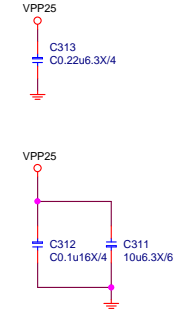
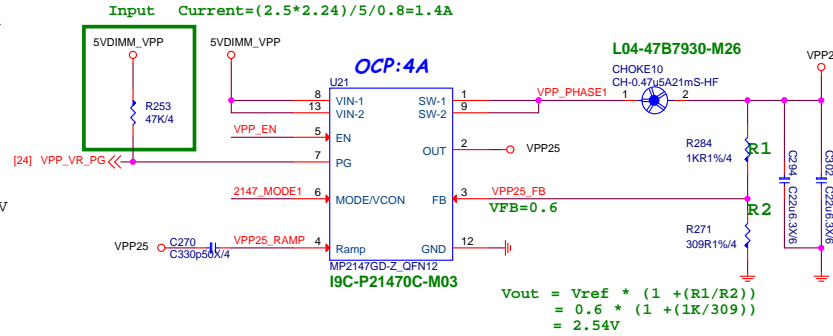
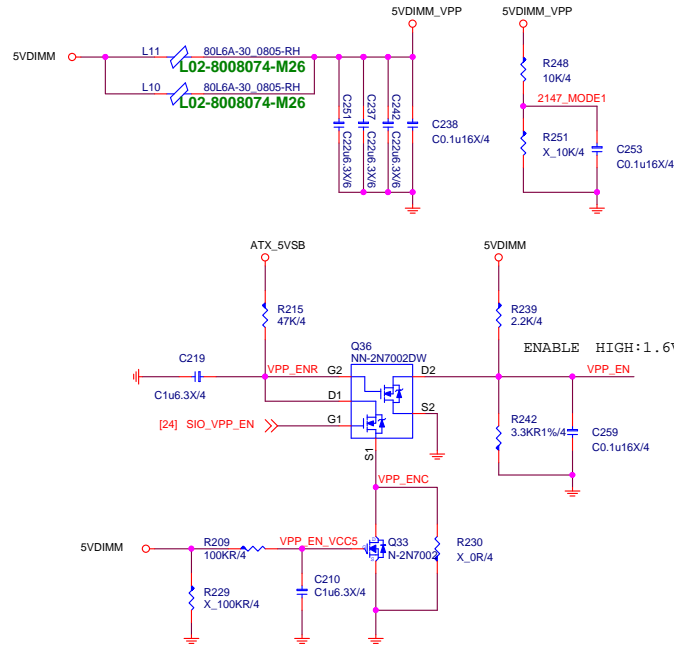


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



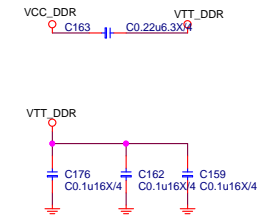
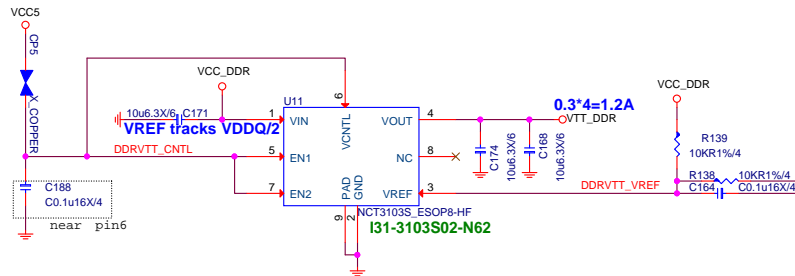
4DIMM : VPP25

2.5V@2.24A

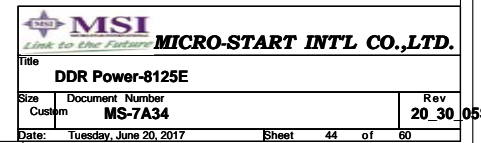


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

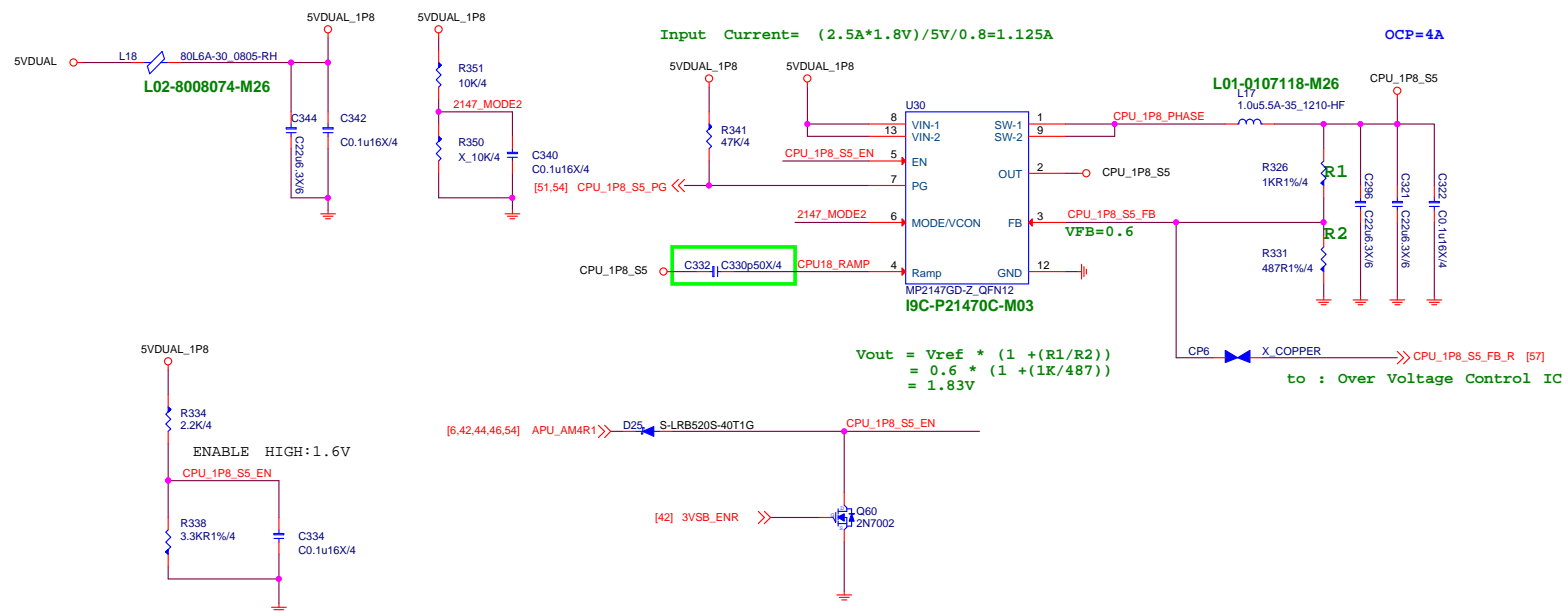


15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT



CPU 1.8V S5 @2.5A

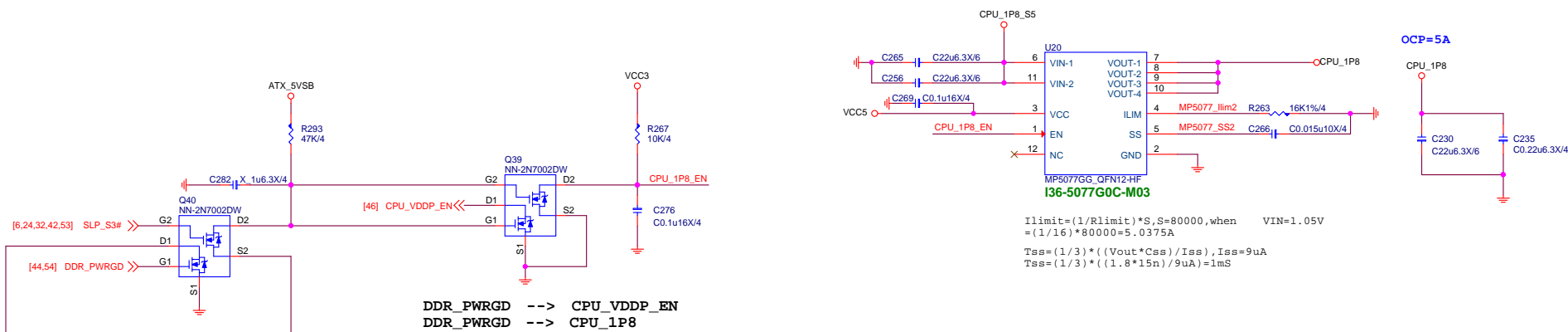
1.8V S5@0.5A
1.8V S0@2A



CPU 1.8V S0

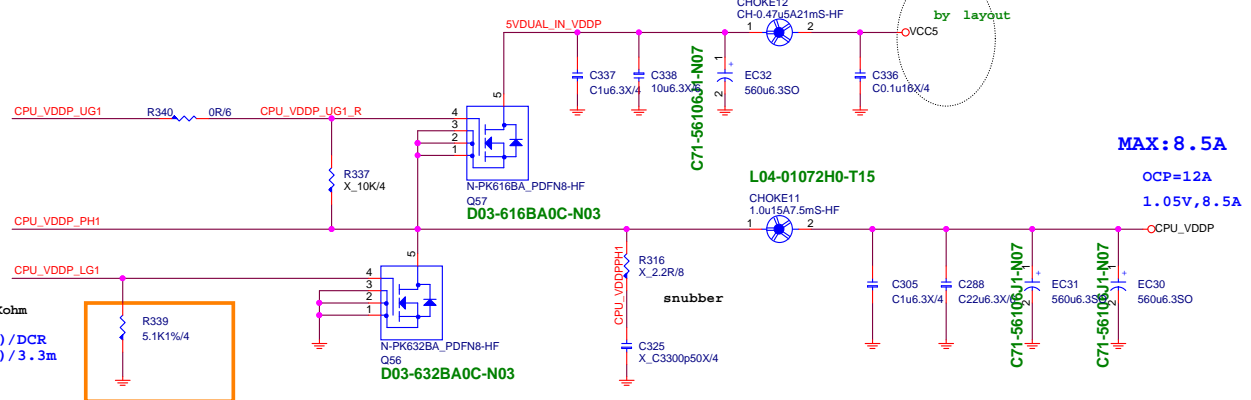
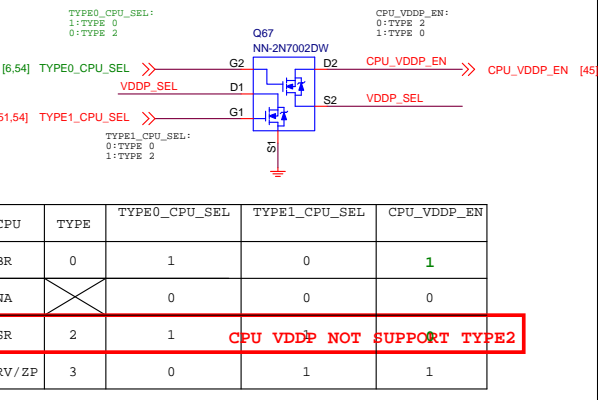
1.8V@2A +0.9A(VCCP_NB_S5) =2.9A

FOR VCCP_SOC@0.9A



S0:8.5A
S5:1A

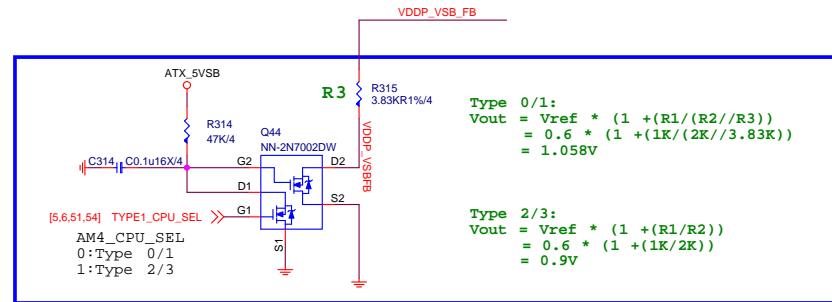
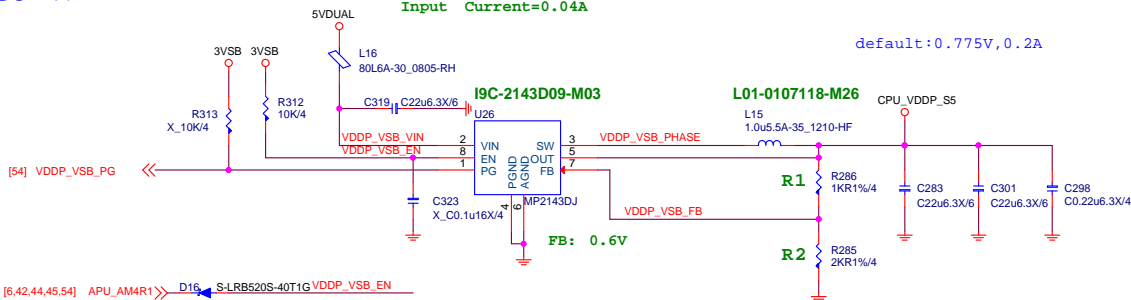
by



(VDDCR_SOC_S5 is only used for AMD TYPE0)

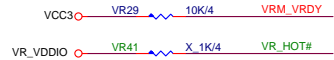
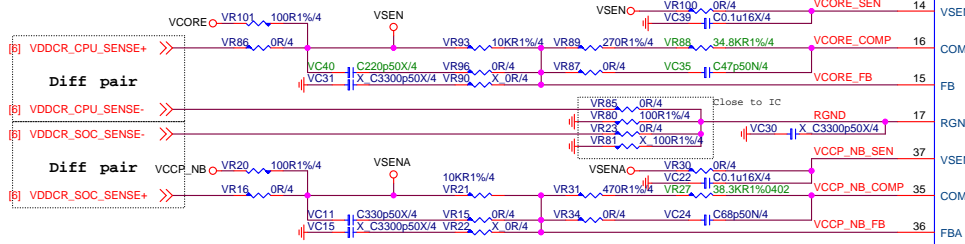
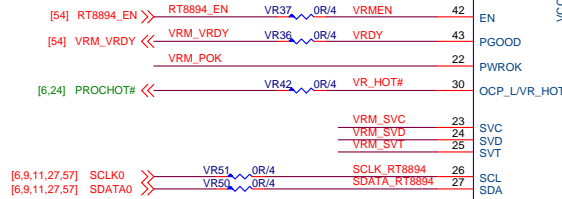
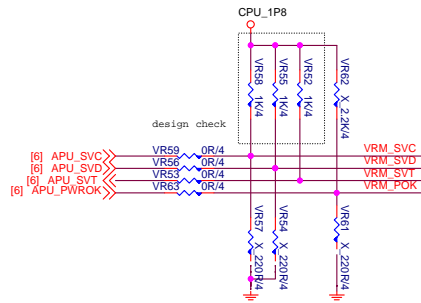
S5:1A

S5:1A

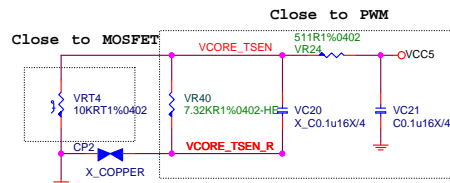


Note:VID Override Circuit

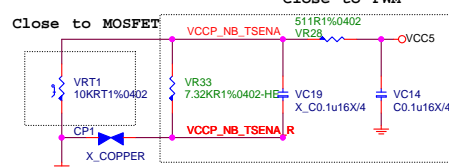
BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



Vcore 1.2V 發壓度恢復

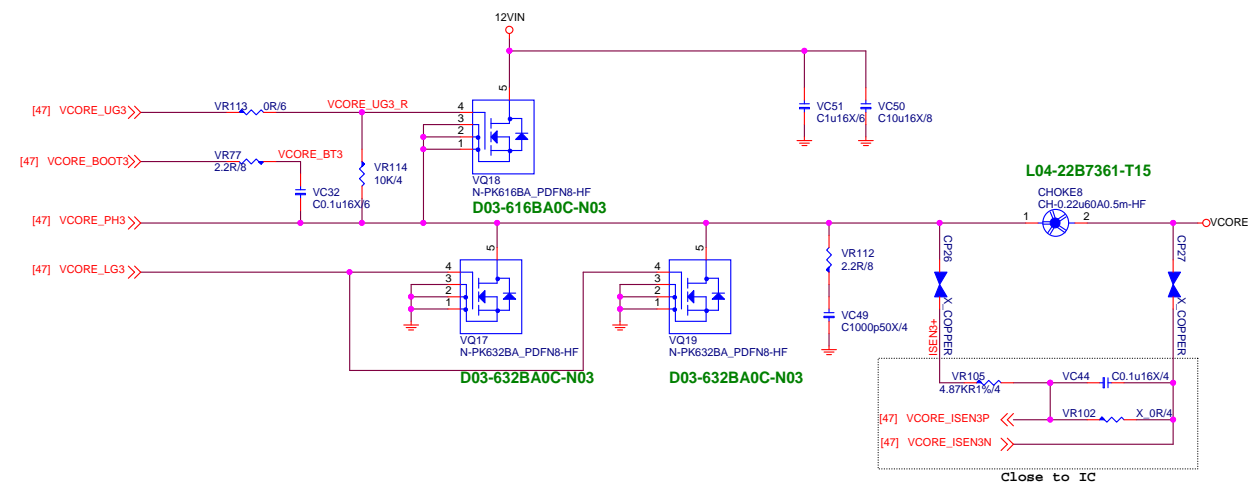
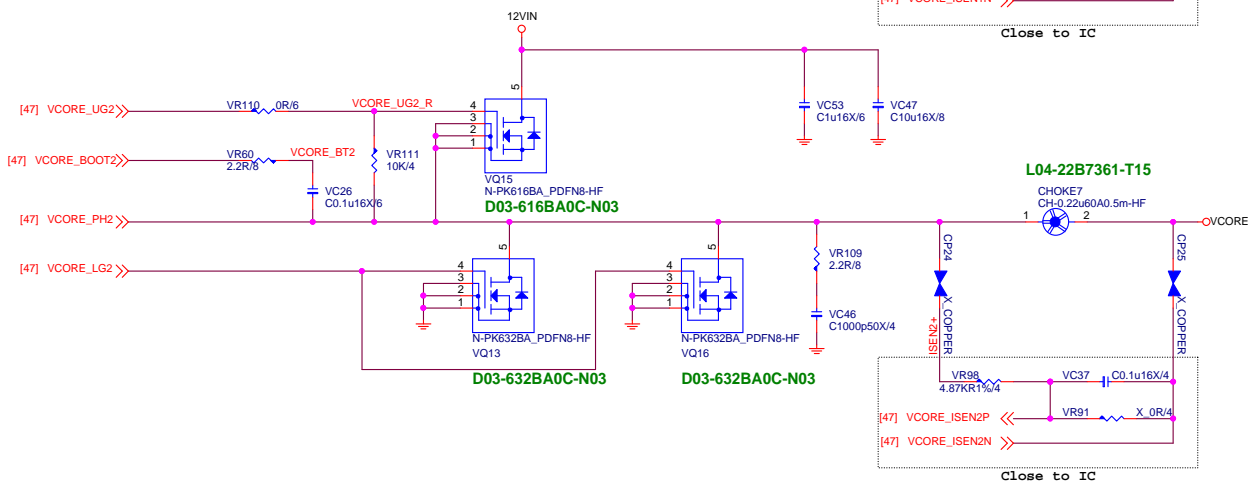
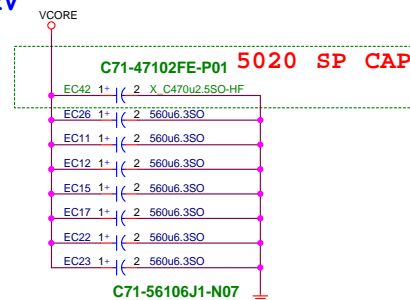
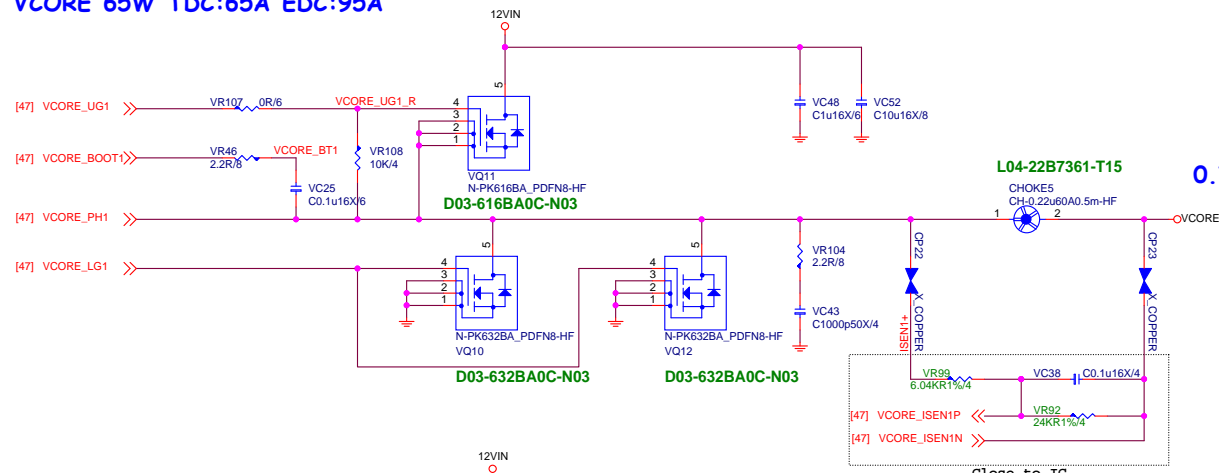


NB項 MOS 溫度會在 124度 VR 拉 1.0V 並恢復恢復

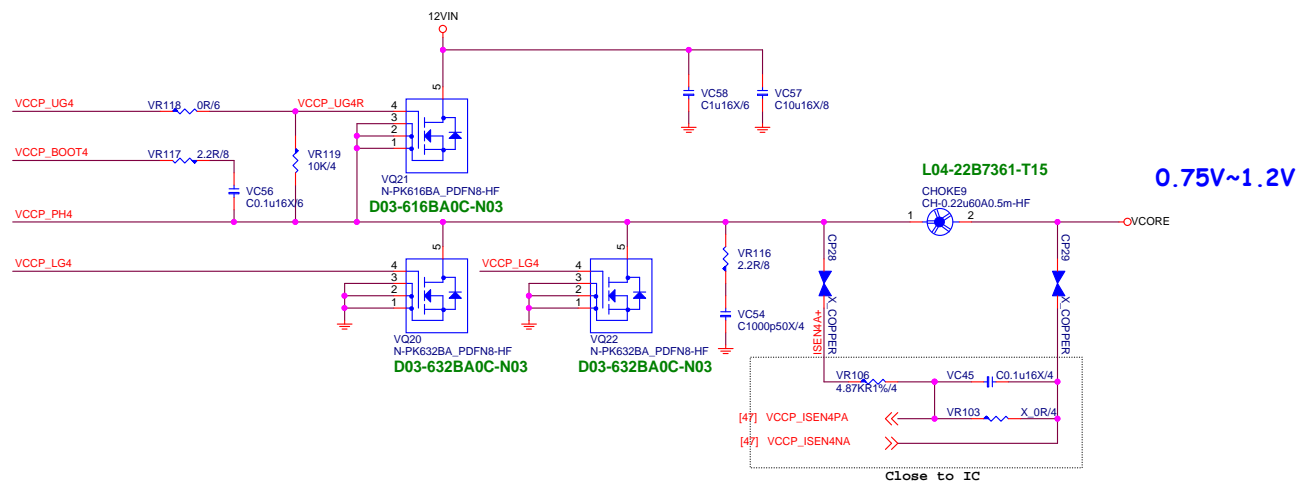


Vinafix.com

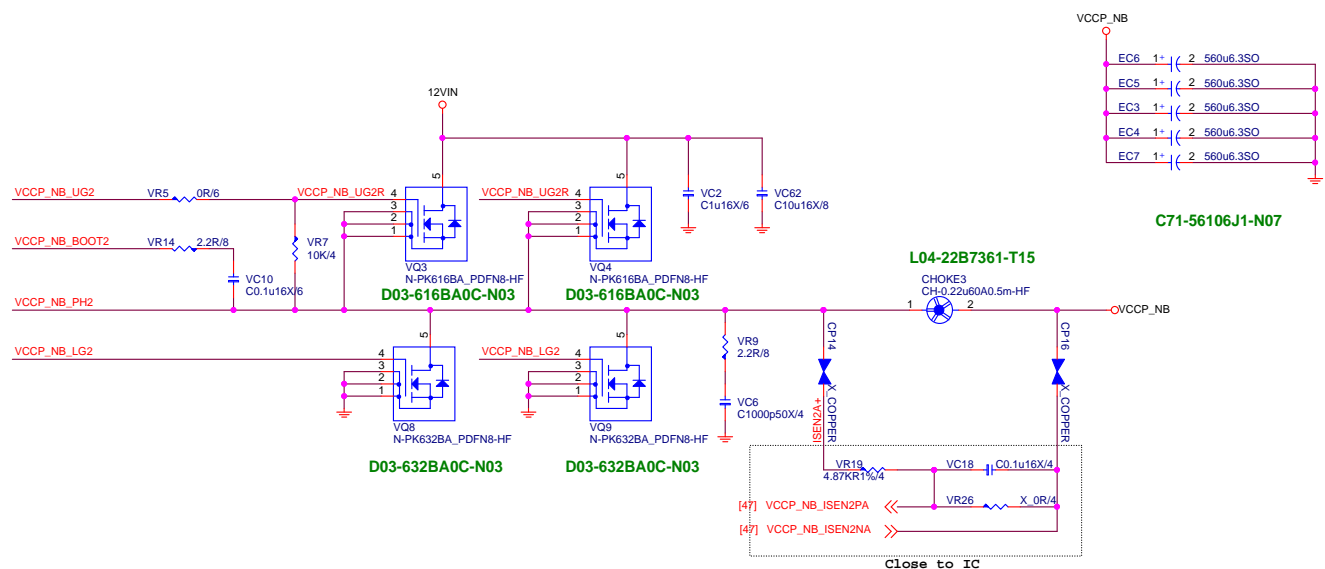
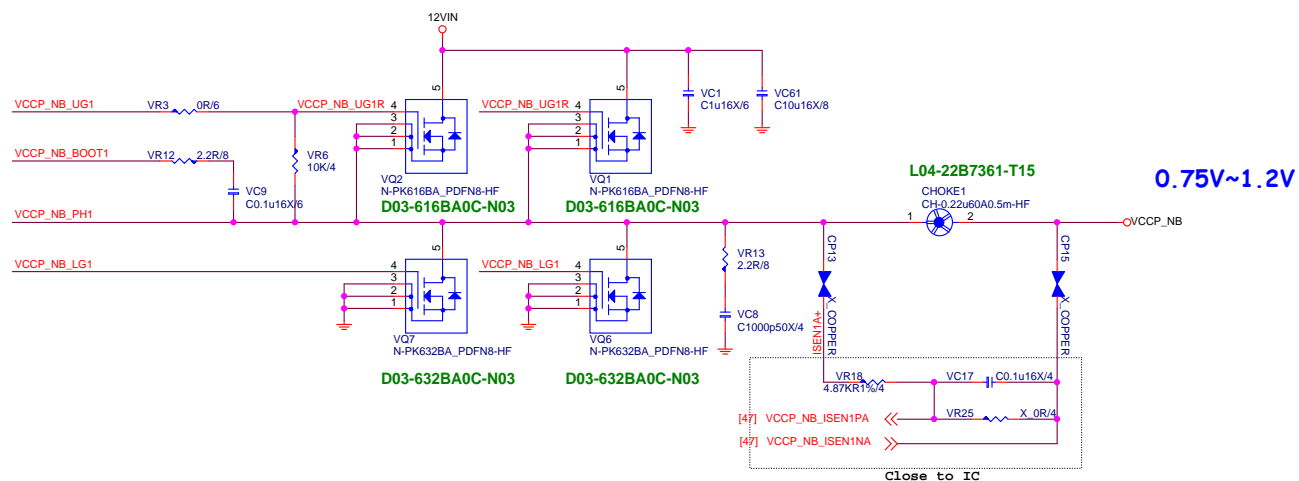
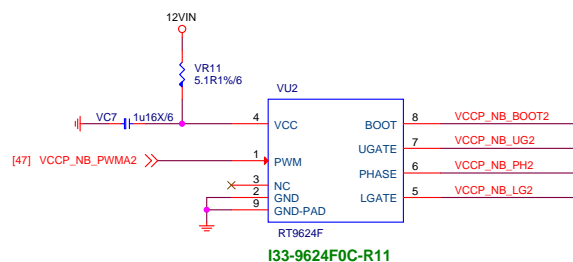
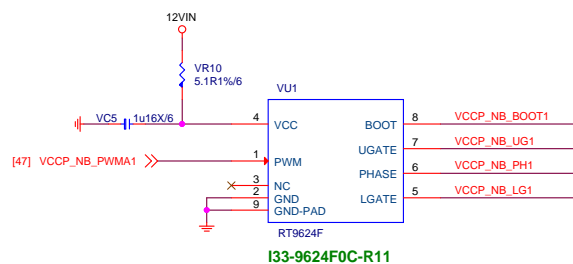
VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A



CPU Power Phase		
Size	Document Number	Rev
Custom	MS-7A34	20_30_05S
Date:	Tuesday, June 20, 2017	Sheet 48 of 60



VCCP_NB 95W TDC:50A EDC:75A
VCCP_NB 65W TDC:50A EDC:75A

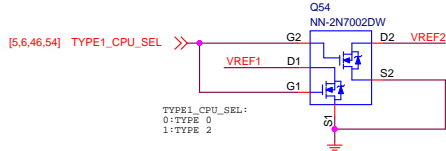
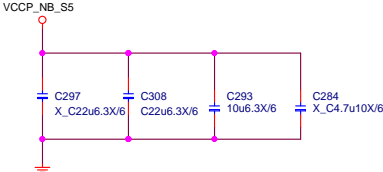
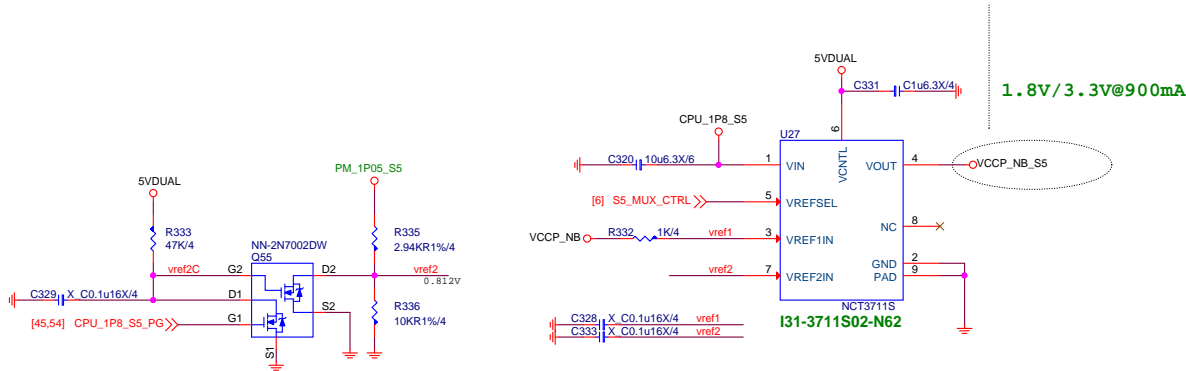


FOR VCCP_SOC_S5
0.9A

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

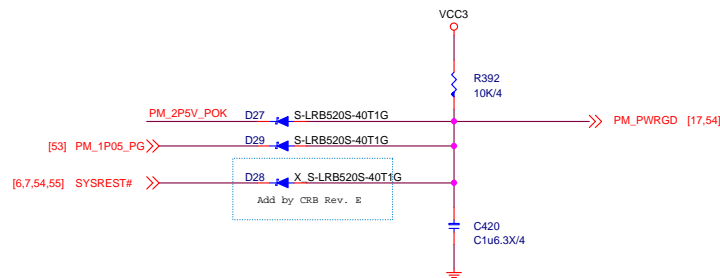
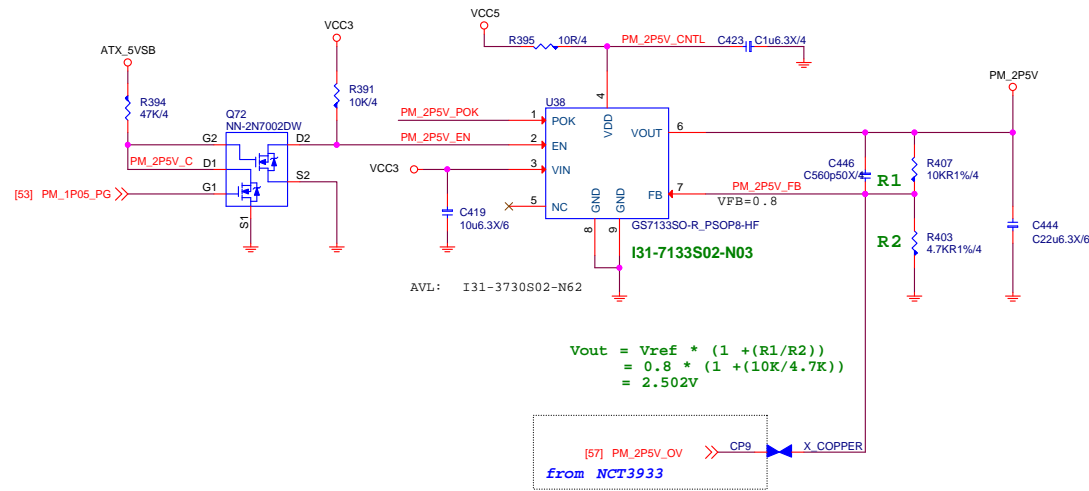
CPU VCCP_NB_S5 ONLY SUPPORT TYPE0



Title			Rev
CPU Power NB Switch			20_30_05S
Size	Document Number		
Custom	MS-7A34		
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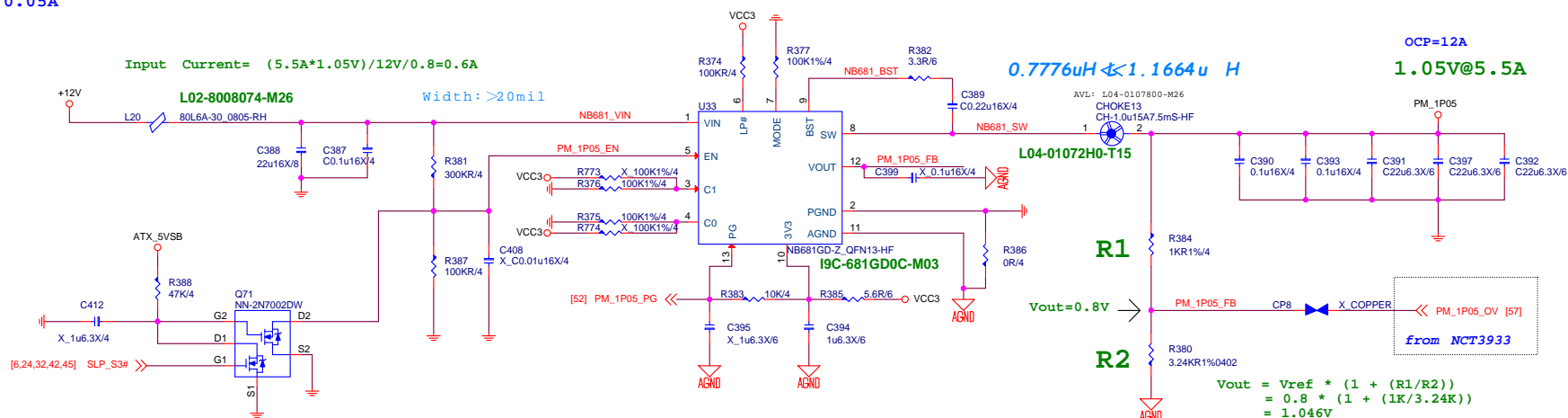
Promontory-2.5V

2.5V@900mA



1.05V
S0:5.5A
S5:0.05A

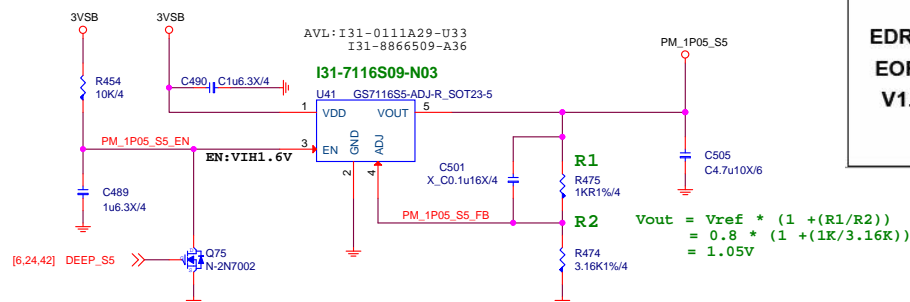
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



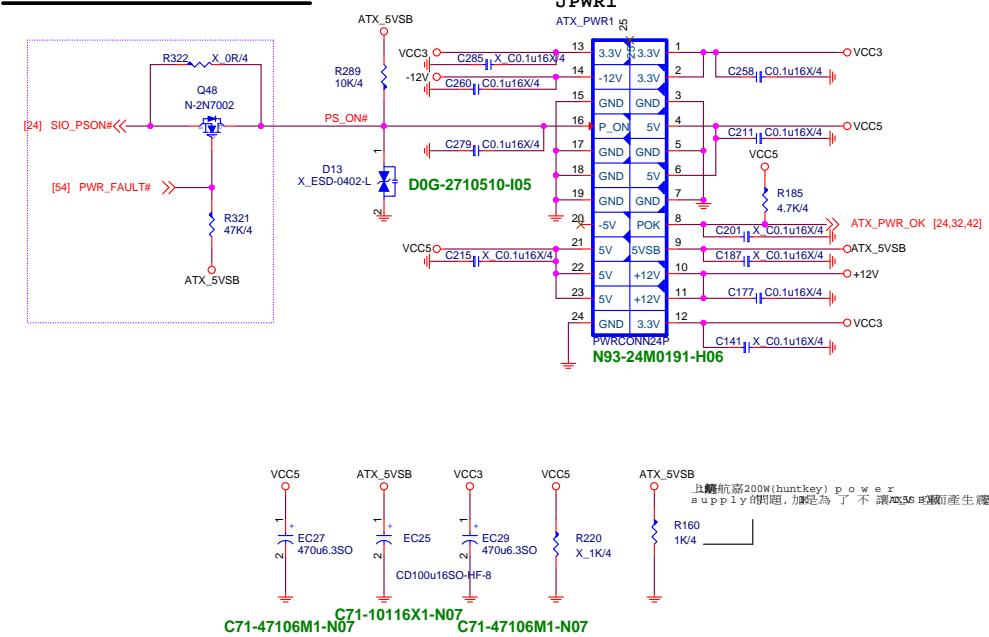
MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPPIO	100 K
M4	Others	150 K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

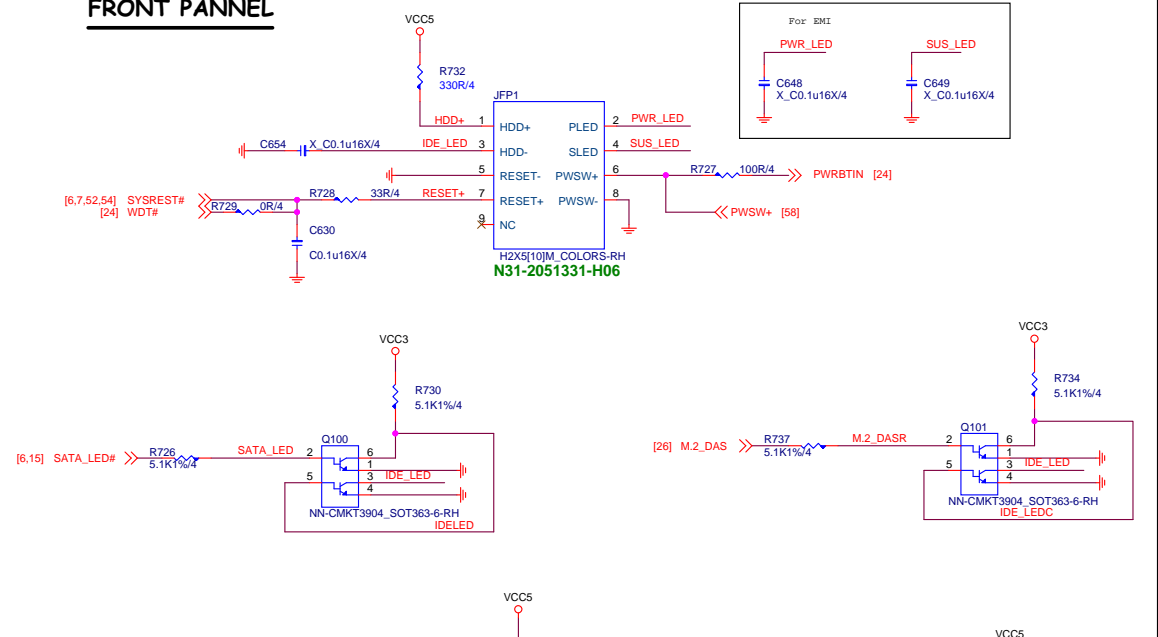
1.05V@0.05A



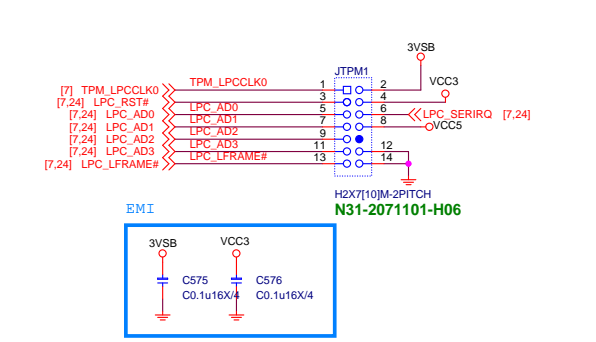
ATX POWER CONNECTOR



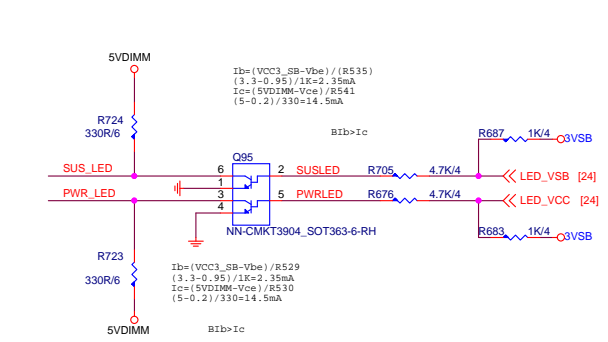
FRONT PANNEL



TPM



LED (for NCT6793D)



Voltage Mearsure Point

VCCORE	1	TP_CPU_CORE
VCCP_NB	1	TP_CPU_NB
CPU_VDDP	1	TP_CPU_VDDP
VCC_DDR	1	TP_VCC_DDR
VTT_DDR	1	TP_VTT_DDR
VPP25	1	TP_VPP25
CPU_1P8	1	TP_CPU_1P8
CPU_1P8_S5	1	TP_CPU_1P8_S5
PM_1P05	1	TP_PM_1P05
PM_1P05_S5	1	TP_PM_1P05_S5
PM_2P5V	1	TP_PM_2P5V
VCCP_NB_S5	1	TP_VCCP_NB_S5
CPU_VDDP_S5	1	TP_CPU_VDDP_S5
CPU_V_1P5V	1	TP_CPU_V_1P5V
5VDIMM	1	TP_5VDIMM
5VDUAL	1	TP_5VDUAL
3VSB	1	TP_3VSB
HDMI_PWR_5V	1	TP_HDMI_PWR_5V
DVI_VGA_5V	1	TP_DVI_VGA_5V
USB30_VCC2	1	TP_USB30_VCC2
USB30_VCC3	1	TP_USB30_VCC3
USB30_TYPEA	1	TP_USB30_TYPEA
USB30_LAN	1	TP_USB30_LAN
USB_PS2_1	1	TP_USB_PS2_1
USB20_VCC2	1	TP_USB20_VCC2
USB20_VCC1	1	TP_USB20_VCC1
5V_FUSB	1	TP_5V_FUSB
5V_RUSB	1	TP_5V_RUSB
VCC3	1	TP_VCC3
VCC5	1	TP_VCC5
+12V	1	TP_+12V
ATX_5VSB	1	TP_ATX_5VSB

MSI
Link to the Future
MICRO-START INTL CO.,LTD.

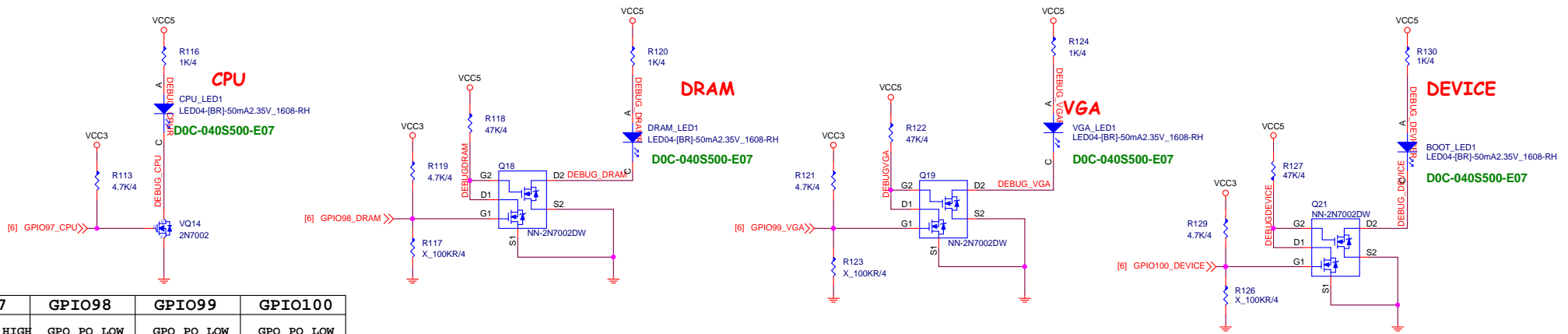
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Size: Custom
Document Number: **MS-7A34**

Date: Tuesday, June 20, 2017
Sheet: 55 of 60

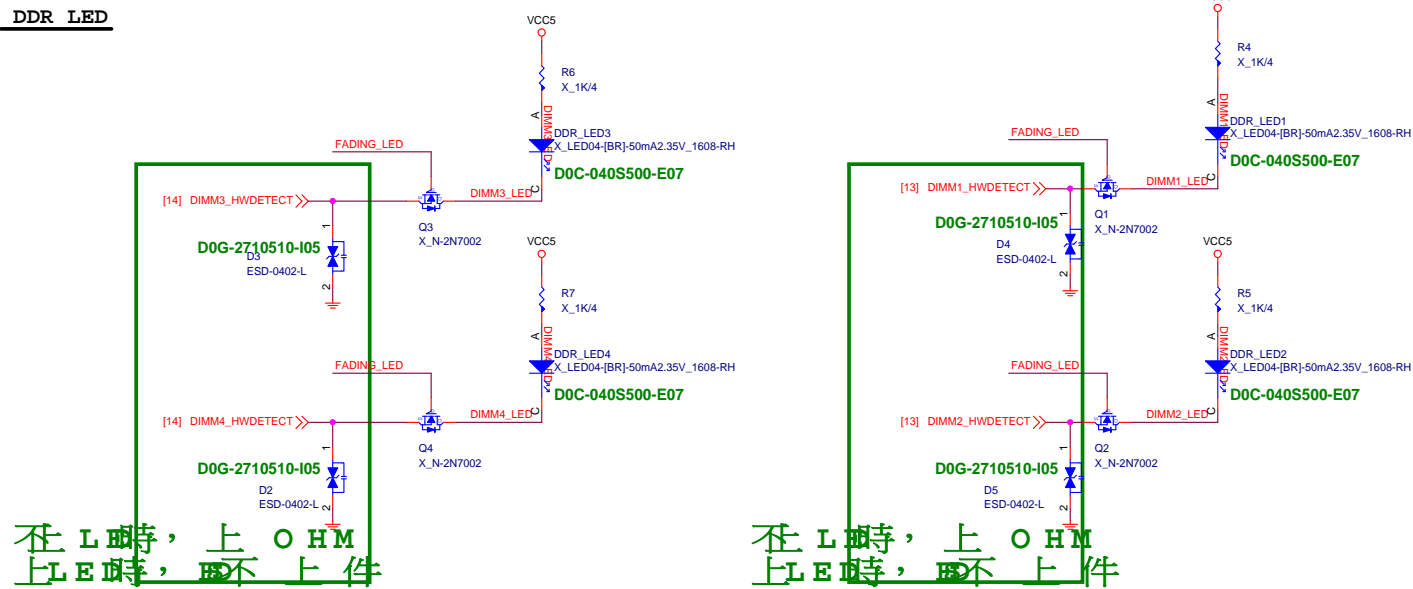
Rev: **20_30_05S**

Debug LED

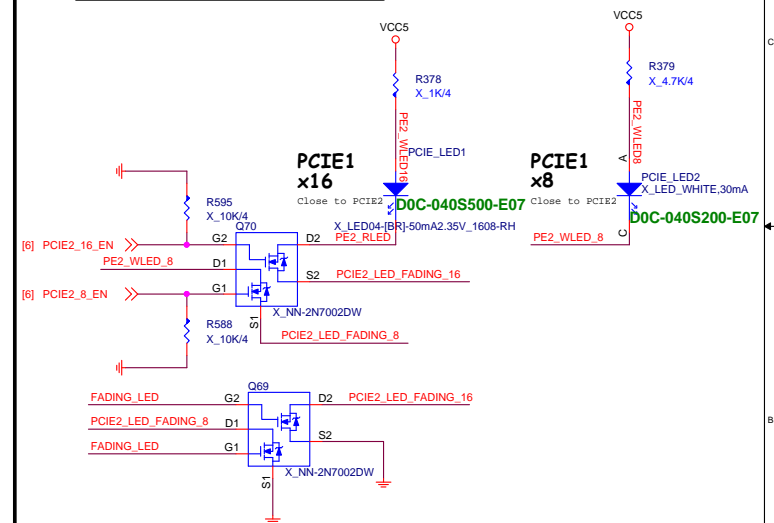


GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

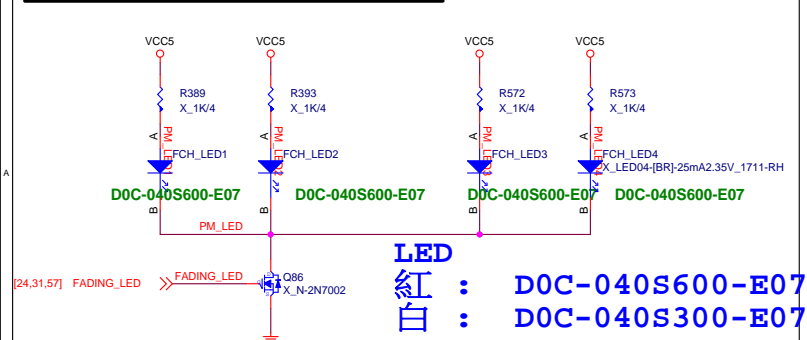
DDR LED



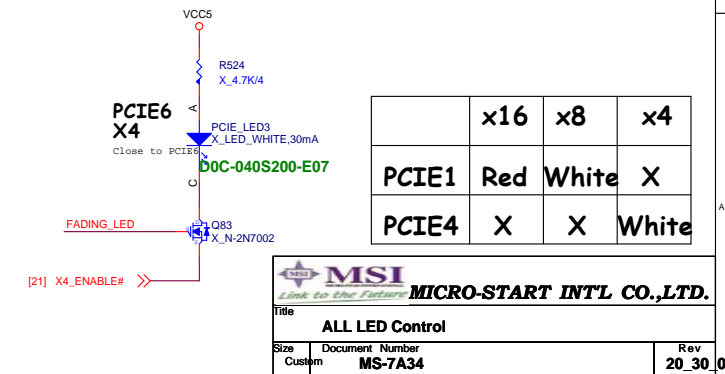
PCI Express LED Control



FCH LED Place under Heat-sink



LED
紅 : D0C-040S600-E07
白 : D0C-040S300-E07



	x16	x8	x4
PCIE1	Red	White	X
PCIE4	X	X	White

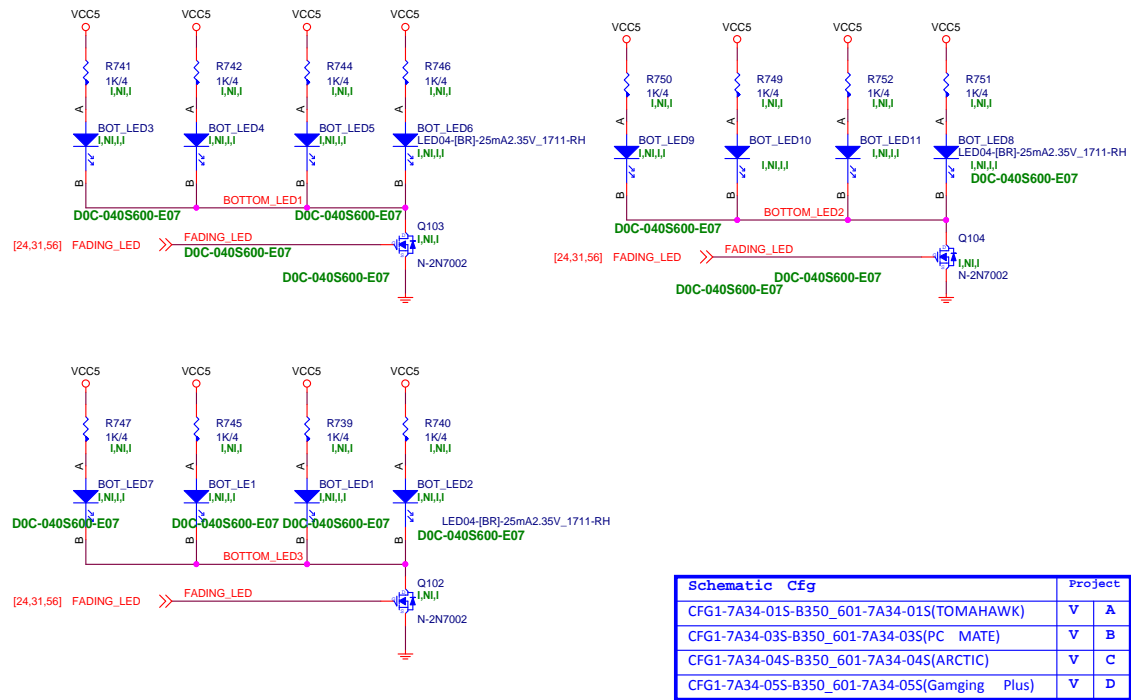
MSI
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Title: ALL LED Control

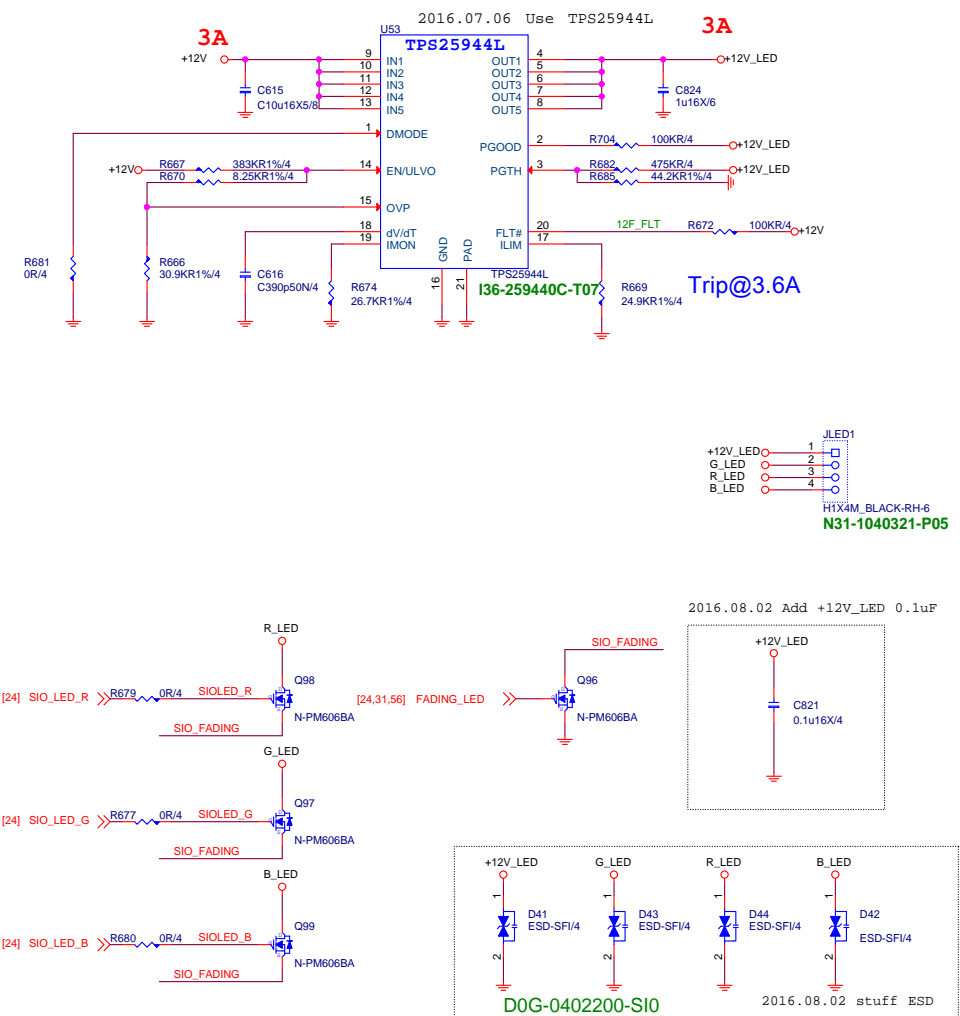
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Date: Tuesday, June 20, 2017 Sheet: 56 of 60

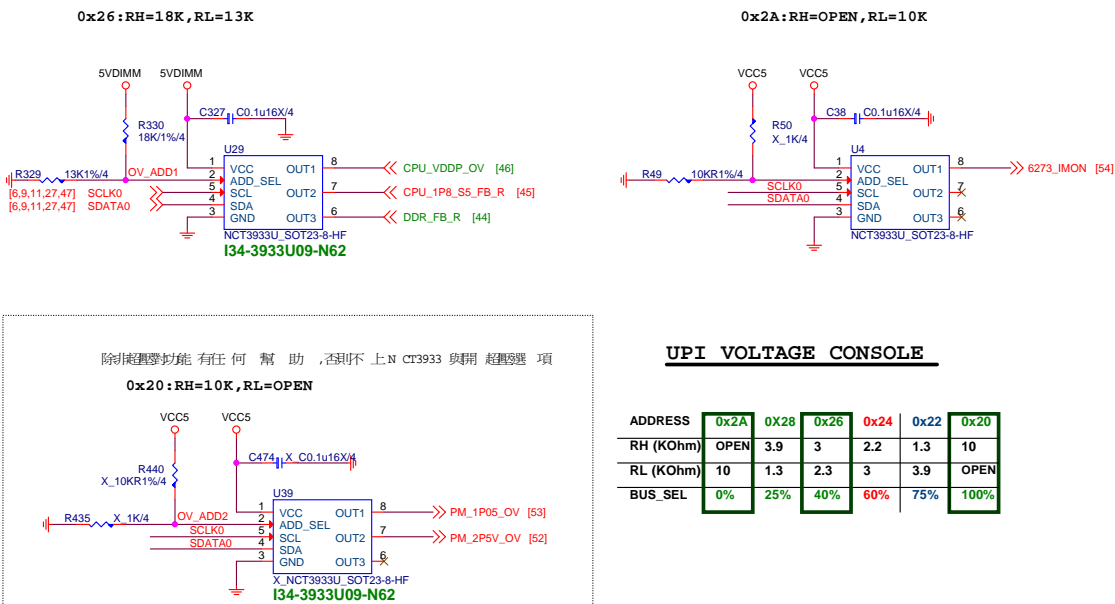
Bottom LED Control by SIO



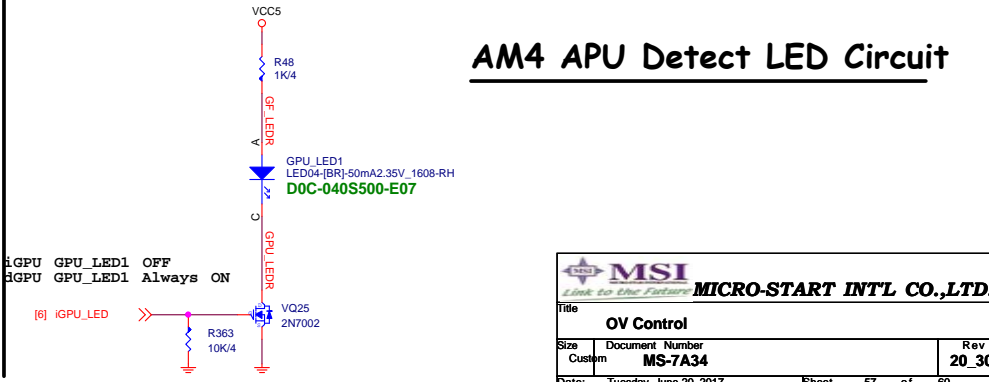
LED Control by SIO




Over Voltage Control IC



AM4 APU Detect LED Circuit



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OV Control

Size Custom

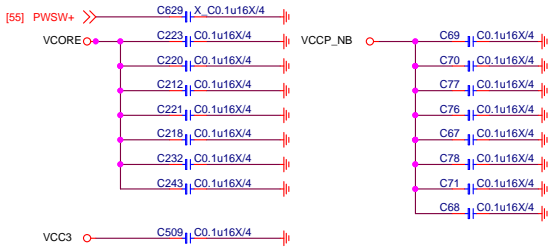
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Rev 20_30_05S

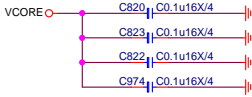
Date: Tuesday, June 20, 2017

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Add for EMI



return path



OPTION BOM PARTS

5010 Level

	TOMAHAWK	PC MATE	ARCTIC	Gaming plus
PCB	OPT_PCB_TOM 7A34-01S Black PD0-07A3410-G37	OPT_PCB_PCM 7A34-02S Black PD0-07A3420-G37	OPT_PCB_ARC 7A34-03S White PS0-07A3430-G37	OPT_PCB_GAP 7A34-04S White PD0-07A3440-G37

FCH	X370_NB B01-2180B5-A08 B01-2180B5-A08 B350_NB B01-2180B5-A08 B01-2180B5-A08	X371	B350
-----	--	------	------

Schematic Cfg	Project
CFG1-7A34-01S-B350_601-7A34-01S(TOMAHAWK)	V A
CFG1-7A34-03S-B350_601-7A34-03S(PC MATE)	V B
CFG1-7A34-04S-B350_601-7A34-04S(ARCTIC)	V C
CFG1-7A34-05S-B350_601-7A34-05S(Gaming Plus)	V D

5020 Level

	TOMAHAWK (A)	PC MATE (B)	ARCTIC (C)	Gaming plus (D)
Bottom LED	OPT_LED_TOM A0110Y001-AR0 LED04[BR]-25mA2.35V_1711-RH D0C-040S600-E07 Red		OPT_LED_ARC A0110Y001-AR0 LED04[PW]-25mA3.2V_1711-HF D0C-040S300-E07 White	OPT_LED_GAP A0110Y001-AR0 LED04[BR]-25mA2.35V_1711-RH D0C-040S600-E07 Red
Audio LED	OPT_AILED_TOM A0110Y001-AR0 LED04[BR]-25mA2.35V_1711-RH D0C-040S600-E07 Red	OPT_AILED_PCM A0110Y001-AR0 LED04[PW]-25mA3.2V_1711-HF D0C-040S300-E07 White	OPT_AILED_ARC A0110Y001-AR0 LED04[PW]-25mA3.2V_1711-HF D0C-040S300-E07 White	OPT_AILED_GAP A0110Y001-AR0 LED04[BR]-25mA2.35V_1711-RH D0C-040S600-E07 Red


FCH LED	DDR_0OHM 0 OHM X_DDR_0OHM R11-0000012-W08
PCH_WLED1 WHITE LED X_PCH_WLED D0C-040S300-E07	

	TOMAHAWK (A)	PC MATE (B)	ARCTIC (C)	Gaming plus (D)
SOLID CAP 100u16	OPT_100u16_TOM B001D-QAP C_P2_5_D6_3_H5 C71-10116X1-N07	OPT_100u16_PCM B001D-QAP C_P2_5_D6_3_H6 C71-10116Q1-A05	OPT_100u16_ARC B001D-QAP C_P2_5_D6_3_H5 C71-10116X1-N07	FOOTPRINT C_P2_5_D6_3_H6 C_P2_5_D6_3_H5 框容
SOLID CAP 270u16	OPT_270u16_TOM B001D-QAP C_P3_5_D8_H8 C71-27117P1-N07	OPT_270u16_PCM B001D-QAP C_P3_5_D8_H9 C71-27117D1-A05	OPT_270u16_ARC B001D-QAP C_P3_5_D8_H8 C71-27117P1-N07	FOOTPRINT C_P3_5_D8_H9 C_P3_5_D8_H8 横包容
SOLID CAP 470u6.3	OPT_470u6.3_TOM B001D-QAP C_P2_5_D6_3_H9_5 C71-47106M1-N07	OPT_470u6.3_PCM B001D-QAP C_P2_5_D6_3_H9 C71-47106K1-A05	OPT_470u6.3_ARC B001D-QAP C_P2_5_D6_3_H9_5 C71-47106M1-N07	FOOTPRINT C_P2_5_D6_3_H9_5 C_P2_5_D6_3_H9 带
SOLID CAP 560u6.3	OPT_560u6.3_TOM B001D-QAP C_P2_5_D6_3_H9_5 C71-56106J1-N07	OPT_560u6.3_PCM B001D-QAP C_P2_5_D6_3_H9 C71-56106F1-A05	OPT_560u6.3_ARC B001D-QAP C_P2_5_D6_3_H9_5 C71-56106J1-N07	FOOTPRINT C_P2_5_D6_3_H9_5 C_P2_5_D6_3_H9 横包容
爾 Typ e A	OPT_TypeA_TOM USBAM_RED-RH-3 USB_A1_9_USB3_1_1 N53-09M0591-L06	OPT_TypeA_PCM USBAM_BLUE-RH-12 USB_A1_9_USB3_1_1 N53-09M0671-L06	OPT_TypeA_ARC USBAM_RED-RH-3 USB_A1_9_USB3_1_1 N53-09M0591-L06	
REAL PS2+USB20	OPT_PS2USB_TOM PS2PS20 MINIDIN_USB2-RH-8 IOASM_USB_DIN14 N58-14M0191-H06	OPT_PS2USB_PCM PS2PS20 MINIDIN_USB2-RH-1 IOASM_USB_DIN14 N58-14M0081-L06	OPT_PS2USB_ARC PS2PS20 MINIDIN_USB2-RH-8 IOASM_USB_DIN14 N58-14M0191-H06	

OPT_PS2USB_TOM1 AVL :N58-14M0211-F02/ N58-14M0191-H06/ N58-14M0241-H06
OPT_PS2USB_PCM1 AVL :N58-14M0081-L06/N58-14M0081-F02/ N58-14M0221-H06

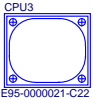
LAN+ U3	OPT_LANU3_TOM LAN+ U3 RJ45_USBX2_LEDX2-1000-RH IOASM_RJ45_USB_LED32 N58-32F0311-F02	OPT_LANU3_PCM LAN+ U3 RJ45_USBX2_LEDX2-TX-RH-93 IOASM_RJ45_USB_LED32 N58-32F0291-F02	OPT_LANU3_ARC LAN+ U3 RJ45_USBX2_LEDX2-1000-RH IOASM_RJ45_USB_LED32 N58-32F0311-F02	
DDR Slot	OPT_DDRSLT_TOM DDRSLT DDRIV-288P_BLACK-RH-21 DDRIV_D288 N13-2880581-L06 Black	OPT_DDRSLT_PCM DDRSLT DDRIV-288P_BLACK-RH-21 DDRIV_D288 N13-2880581-L06 Black	OPT_DDRSLT_ARC DDRSLT DDRIV-288P_WHITE-RH-7 DDRIV_D288 N13-2880541-L06 White	OPT_DDRSLT_GAPB DDRSLT DDRIV-288P_BLACK-RH-21 DDRIV_D288 N13-2880581-L06 Black
Audio	OPT_AUDIO_TOM AUDIO JACK-AUDIOX6F_B/LB/LB/RED/BL-RH AUDIO_JACK6_26P_U2 N54-26F0361-L06 Black\Red	OPT_AUDIO_PCM AUDIO JACK-AUDIOF_B/LB/UR/GR/GY/RED-RH AUDIO_JACK6_26P_U2 N54-26F0351-L06 Color	OPT_AUDIO_ARC AUDIO JACK-AUDIOX6F_B/LB/LB/RED/BL-RH AUDIO_JACK6_26P_U2 N54-26F0361-L06 Black\Red	FOOTPRINT AUDIO_JACK6_26P_U2 JACK_AUD_D26P 横包容
PCH SINK	OPT_PCHSINK_TOM PCH SINK E31-0408600-A87	OPT_PCHSINK_PCM PCH SINK E31-0408870-K08	OPT_PCHSINK_ARC PCH SINK E31-0408880-A87	OPT_PCHSINK_GAP PCH SINK E31-0408880-A87
MOS heatsink(short)	OPT_MOS_ST_TOM MOS-ST E31-0504280-A87	OPT_MOS_ST_PCM MOS-ST E31-0504720-K08	OPT_MOS_ST_ARC MOS-ST E31-0504730-A87	OPT_MOS_ST_GAP MOS-ST E31-0504730-A87
MOS heatsink(Long)	OPT_MOS_LO_TOM MOS-LO E31-0504270-A87	OPT_MOS_LO_PCM MOS-LO E31-0504710-K08	OPT_MOS_LO_ARC MOS-LO E31-0504700-A87	OPT_MOS_LO_GAP MOS-LO E31-0504700-A87
PCIEx16	OPT_PCIE16_TOM PCIE-16 Black N11-1641491-L06	OPT_PCIE16_PCM PCIE-16 Black N11-1641491-L06	OPT_PCIE16_ARC PCIE-16 White N11-1641601-L06	OPT_PCIE16_GAP PCIE-16 Red N11-1641671-L06
PCIEx4	OPT_PCIE4_TOM PCIE-4 Black N11-1000151-L06	OPT_PCIE4_PCM PCIE-4 Black N11-1000151-L06	OPT_PCIE4_ARC PCIE-4 Black N11-1000151-L06	OPT_PCIE4_GAP PCIE-4 Red N11-1000231-L06

X370	X370_MKTGname G51-M1SPK15-Q13	B350_MKTGname G51-M1SPK15-Q13	B350_LABEL_PCM N11,N11 G51-M1SPK89-Q13	B350_LABEL_ARC N11,N11 G51-M1SPK89-Q13	B350_LABEL_GAP N11,N11 G51-M1SPK89-Q13
B350	G51-M1SPK14-Q13	G51-M1SPK14-Q13	G51-M1SPK89-Q13	G51-M1SPK89-Q13	G51-M1SPK89-Q13

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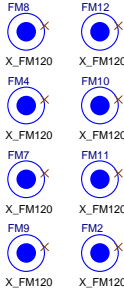
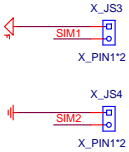
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Size	Document Number			Rev	
Custom	M5-7A34			20_30	05S
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CPU Socket

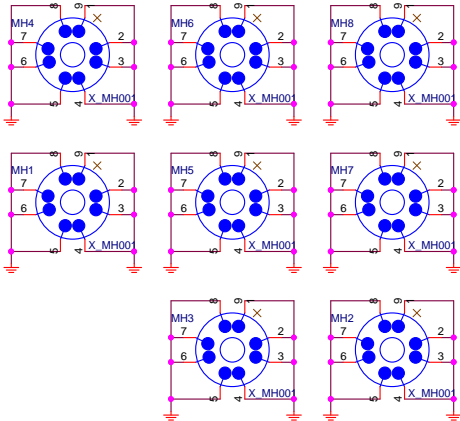


E95-0000021-C22

Simulation



Optics Orientation Holes



MANUAL PART

UEFI1
G51-M1SPXXA-A09

G51-M1SPXXA-A09

HDMI_LA1
Label
HDMI
HDMI LABEL

Y01-RHDMI03-000



AVL1:
D06-0100161-P52
D06-0100101-K26

cFosSoftware [N,I]

Y02-MU00170-CFO

Y02-MU00170-CFO

NAHIMIC [N,I]

Y02-MU00100-NAH

Y02-MU00100-NAH

XSPLIT [N,I]

Y02-MA00401-XSP

Y02-MA00401-XSP

SSE [N,I]

Y02-MA00101-SSE

Y02-MA00101-SSE

VRREADY COVER1

VR
READY

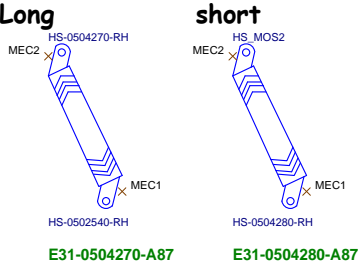
X1

K E21-7976010-RH

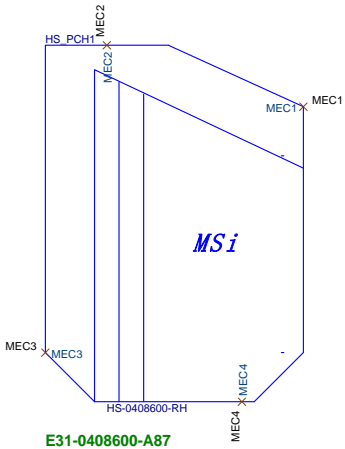
E21-7A63020-A91

Schematic Cfg	Project	
CFG1-7A34-01S-B350_601-7A34-01S(TOMAHAWK)	V	A
CFG1-7A34-03S-B350_601-7A34-03S(PC MATE)	V	B
CFG1-7A34-04S-B350_601-7A34-04S(ARCTIC)	V	C
CFG1-7A34-05S-B350_601-7A34-05S(Gamging Plus)	V	D

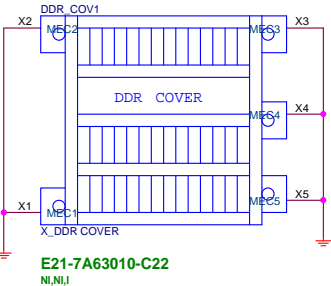
MOS SINK




PCH SINK



DDR Cover



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Title Manual Parts			
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